Future Industrial Infrastructure Distribution Systems Consortium

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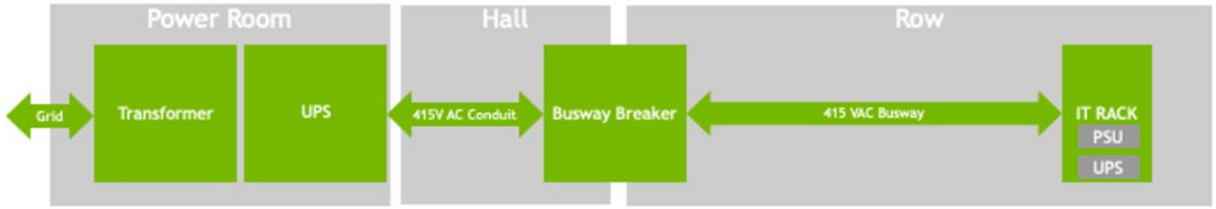
Motivation for DC Data Centers

- **Scalable:** 100 kW–1 MW+ racks on same backbone
- **Efficient:** Up to 5% better than 54 V
- **Less Copper:** Lower current → less copper & heat
- **Reliable:** Centralized conversion reduces PSU failures
- **Cooler Racks:** Frees space, lowers thermal stress
- **Future-Proof:** Supports 1 MW+ next-gen racks



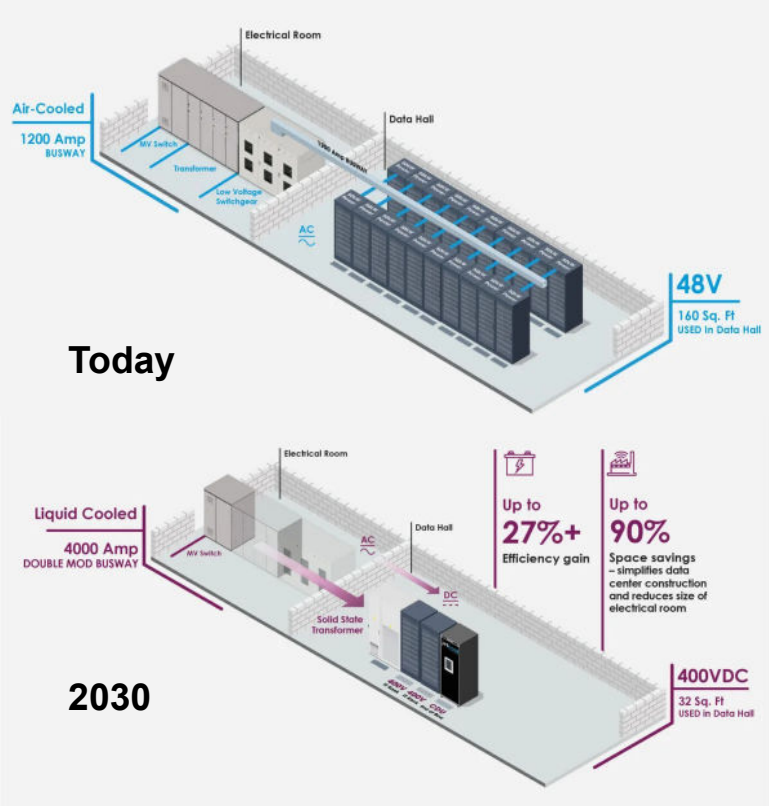
Current datacenter architecture [1]

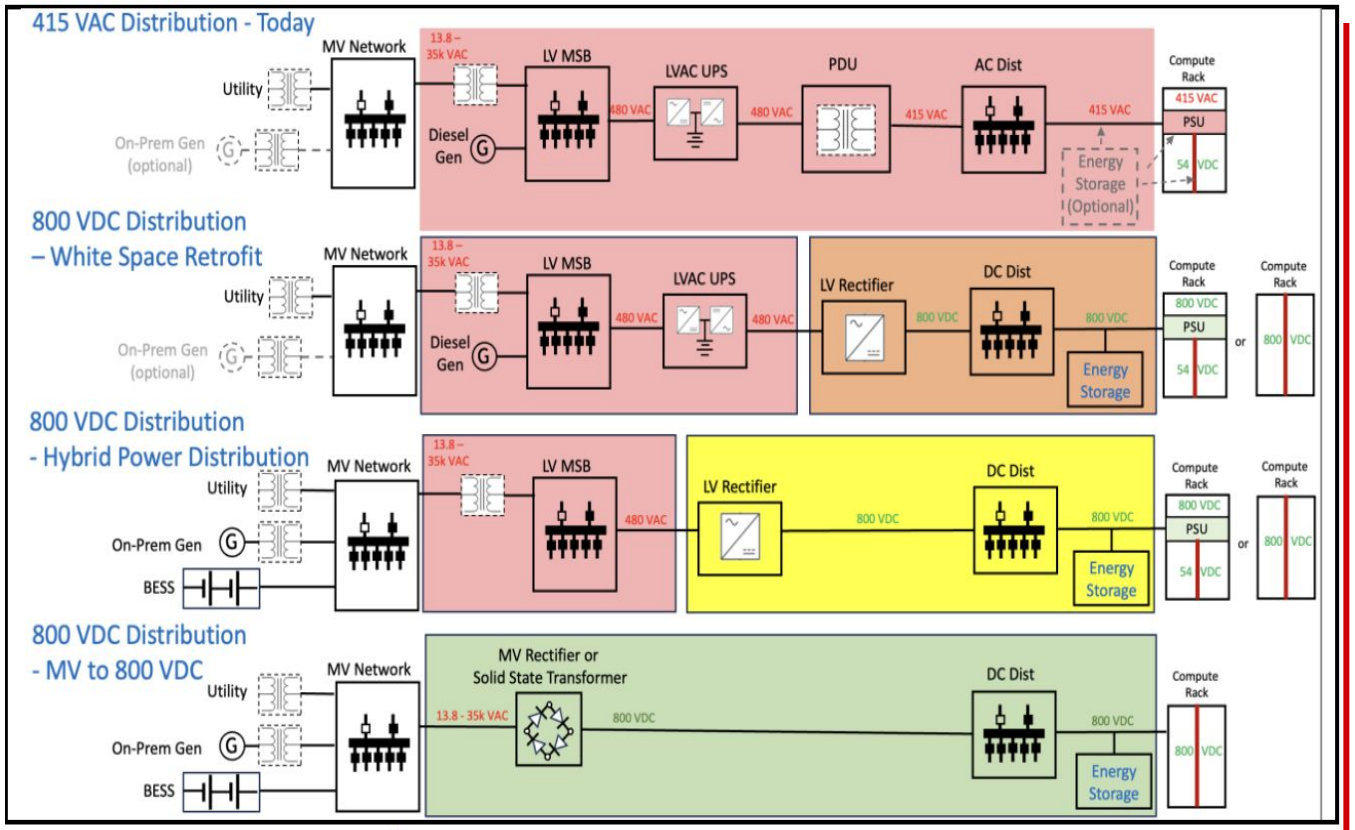
NVIDIA 800 VDC architecture minimizes energy conversions [1]

Metric	NVIDIA GB300 NVL72	NVL576 Rubin Ultra (Rubin Ultra NVL576)
Generation / Architecture	Blackwell Ultra (GB300)	Rubin Ultra (next-gen)
Number of GPUs per Rack	**72 Blackwell** Ultra GPUs	Up **to 576 Rubin Ultra** GPUs
CPU / Accompanying Processors	36 Grace CPUs (Arm)	Vera CPU (88-core custom Arm)
Power Consumption	~**120.8 kW**) per rack Supermicro spec: 132 kW (8 × 1U 33 kW PSUs)	~**600 kW** per rack (liquid-cooled "Kyber" rack)
Voltage / Power Delivery	- Supports **208V / 60 Hz, 415V / 50–60 Hz, 480V / 60 Hz**.	**800 VDC**
Performance (Speed Improvement)	"**1.5× more dense FP4 compute**" over prior architectures.	**~14× the performance** (FP4 inference) compared to GB300 NVL72.

[1] https://developer.nvidia.com/blog/nvidia-800-v-hvdc-architecture-will-power-the-next-generation-of-ai-factories/
[2] https://developer.nvidia.com/blog/building-the-800-vdc-ecosystem-for-efficient-scalable-ai-factories/

Data Center Evolution Towards DC





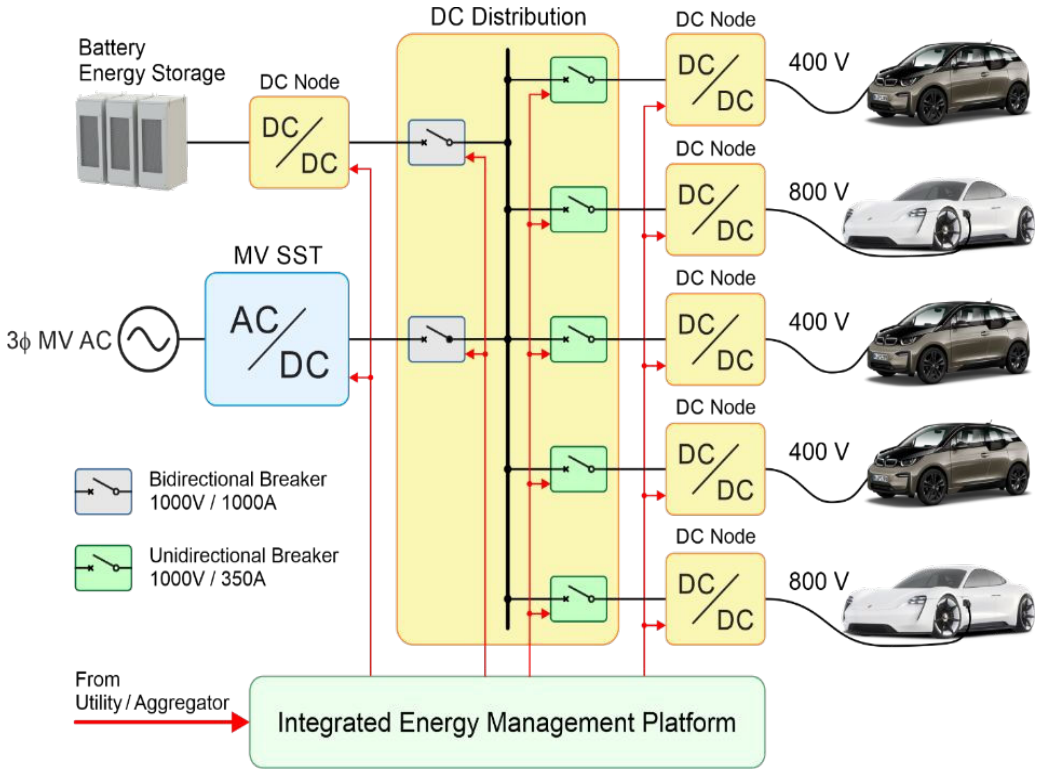
Proposed datacenter architecture evolution – NVIDIA[3]

[3] J. Huntington & M. Tu, "800 VDC Architecture for Next-Generation AI Infrastructure", https://nvdam.nvidia.com/assets/share/asset/zlg5snufeo

Intelligent, Grid-Friendly, Modular Extreme Fast Charging System with Solid-State Direct-Current Protection

Develop and deploy a 1 MW medium voltage XFC station:

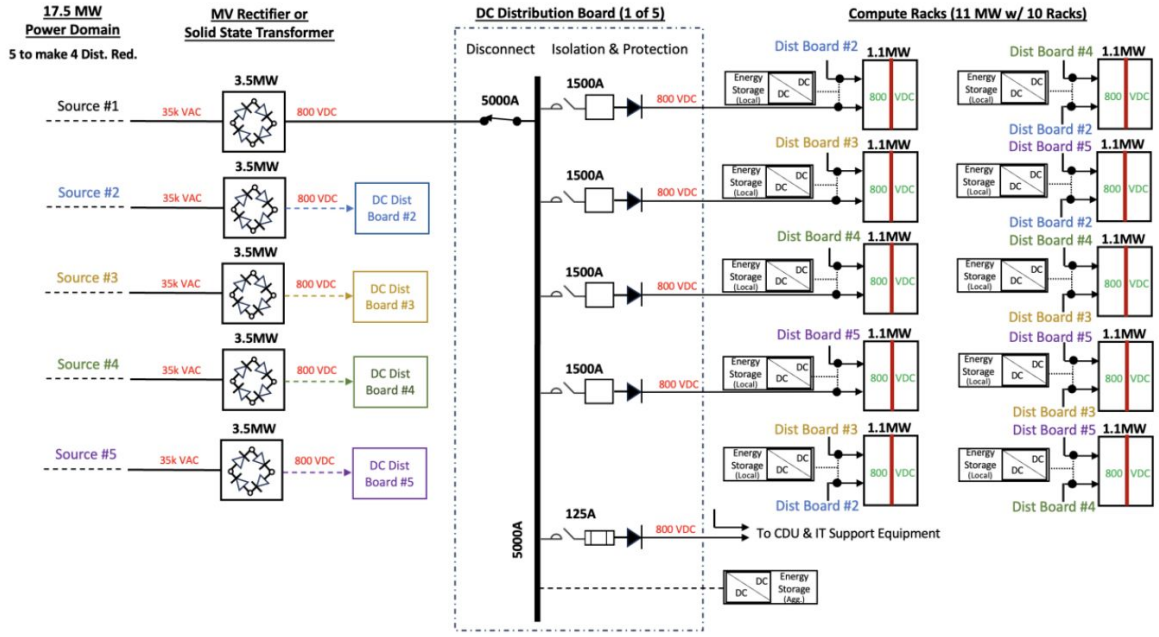
- Shared bi-directional Solid-State Transformer (SST) connecting directly to the medium voltage (MV) distribution system
- DC distribution network with solid-state DC protection



SST-Based Data Center Challenges

Power-Electronics–Intensive Distribution Challenges

- Multi-vendor converters can interact in unexpected ways causing system instability
- Compute loads fluctuate rapidly, stressing system components and complicating system protection
- DC protection design and coordination is not settled
- Desired component behavior during faults may be protection scheme specific



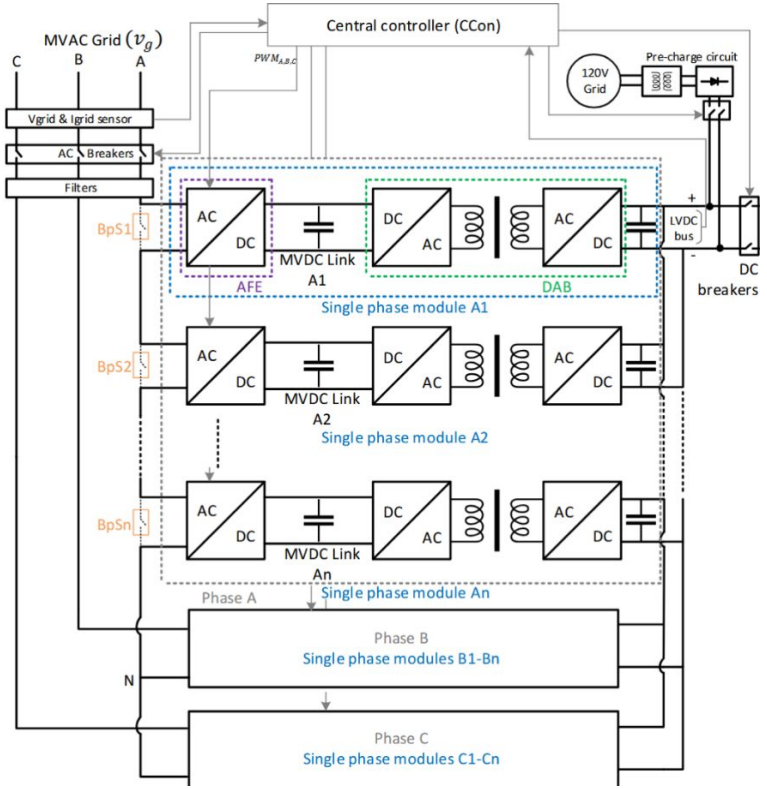
Converter Response

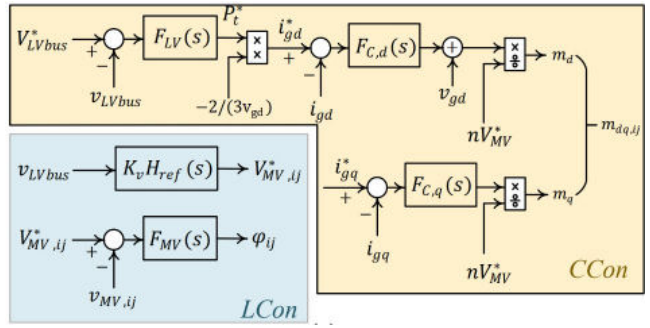
Key Drivers of Converter Response

- Capacitor sizing and ride-through settings strongly influence fault current magnitude and duration.
- Control loop design determines:
  - Dynamic response
  - Stability margins
  - Interaction with upstream and downstream devices

Critical Design Questions

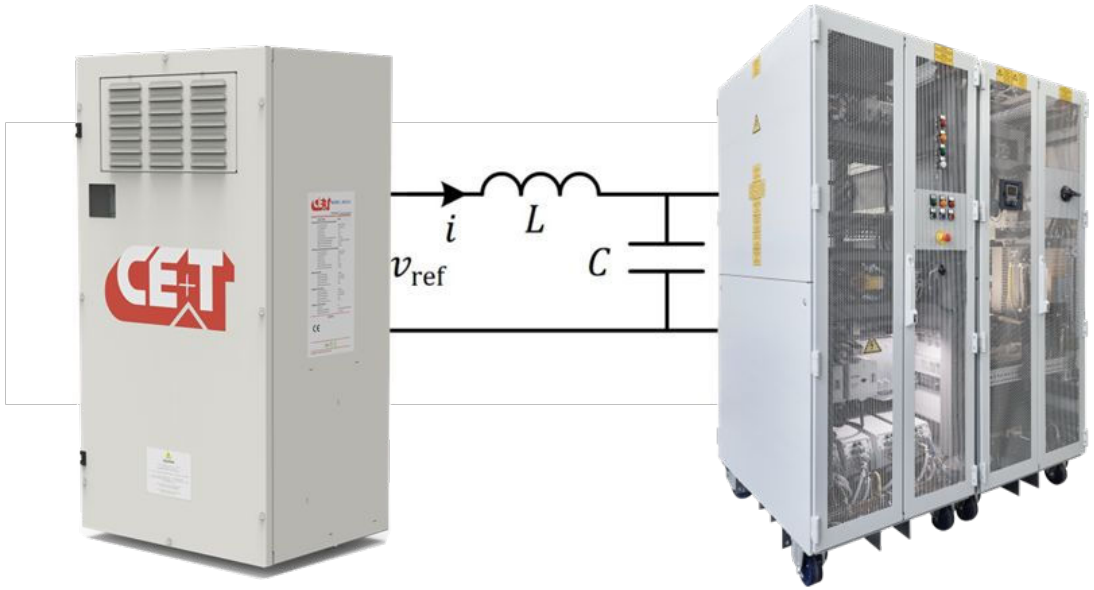
- How do you design a power converter to interact in a stable way within a larger system?
- What information about the converter is needed to properly understand component-to-component interactions?
  - Control bandwidth and structure
  - Small and large signal behavior
  - Ride-through behavior

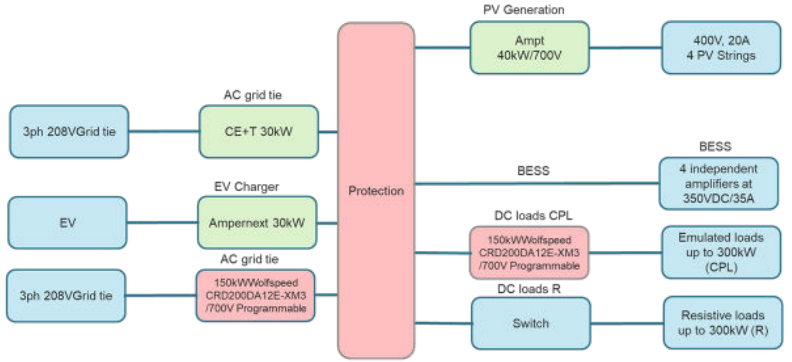




Sample Characterization: CPL Instability

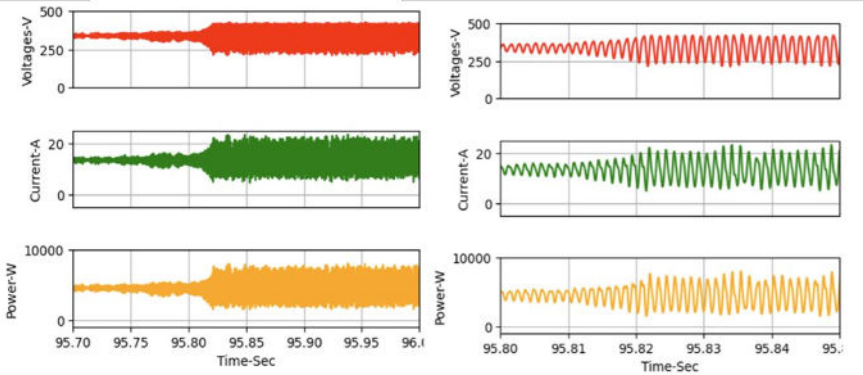
- Based on designed LC parameters and droop, CPL instability is calculated.
  - Stabiliti 30C3 CE+T COTS - as source converter.
  - EGSTON CSU100 Amplifier - as CPL converter.





Grid parameters				
V_n(V)	K	L(mH)	C_{base}(uF)	P(kW)
350	1	0.76	30.8	4.6

$$C_{base} = {}^{L}/_{KR_e}$$



Anees, M., Qi, L., Khan, M., and Lukic, S. (2024). A baseline approach for modeling and characterization of commercial off-the-shelf (cots) droop-controlled converter. In IECON2024 - 50th Annual Conference of the IEEE Industrial Electronics Society, pages 1–7, Chicago, IL, USA

Research Approach

Overarching Goal: Integrate hardware design, control, protection, and stability assessment into a unified framework that forms the foundation for the evaluation of DC infrastructure

- **Component Modeling:** Develop and validate models of converters and loads to identify interaction-induced instabilities.
- **Component characterization:** Develop a platform that extracts critical component behavior that allow precise component modeling.
- **System-Level Topology and Control Development:** Establish a framework to design and evaluate control, topology, and protection architectures.
- **Integration and Standardization:** Develop an Interoperability Data Model capturing component behavior that can help drive system level design decisions.

Statement of Work

1. Define system-level architectural advantages of DC vs. AC for AI data centers, with a focused analysis of the Kyber rack and its implications for overall AI data center architecture.
2. Develop and validate high-fidelity simulation models for representative DC infrastructure components and architectures using an existing hardware testbed.
3. Establish systematic methods for analyzing small-signal and large-signal stability in DC systems, including converter-to-converter and converter-to-load interactions.
4. Propose hierarchical and distributed control strategies that enable coordinated operation across multiple converters and subsystems.
5. Integrate control, protection, and stability assessment into a unified framework that forms the foundation for standardized design and evaluation of DC infrastructure

Team

- **Srdjan Lukic,** Lampe Distinguished Professor, Electrical and Computer Engineering; Deputy Director, FREEDM Center
  - Research Focus on power electronics design and control
  - Lead on Microgrid Control/Coordination Co-Design (MicroC3) and SST development projects
- **Ayman AlZawaideh,** Ph.D. student in Electrical Engineering
  - Graduate researcher contributing modeling, simulation, and experimental validation on Microgrid Control/Coordination Co-Design (MicroC3)
- **Muhammad Anees** Ph.D. student in Electrical Engineering
  - Research focus on DC microgrids, converter control, and stability analysis