"Advancing Power Electronics & Packaging Including AI/ML/DT Reliability Integration"

Prof. Doug Hopkins, ECE and Prof. Jong Ryu MAE

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Prof. Doug Hopkins, ECE, Director
Prof. Jong Ryu, MAE, Assoc Dir.

MIND Multiphysics Multiscale Intelligent Design
Prof Jong Ryu, MAE Director

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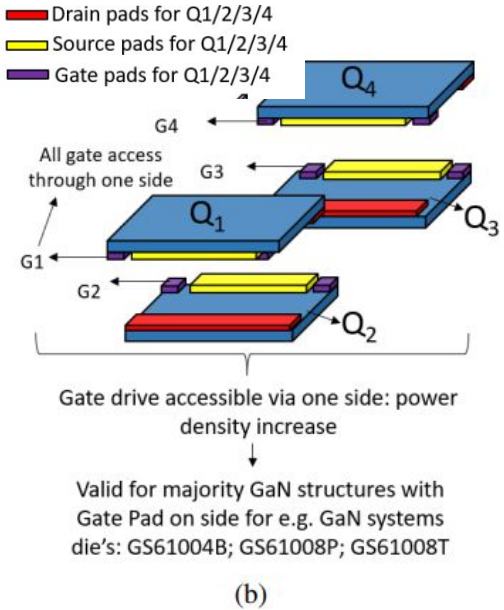
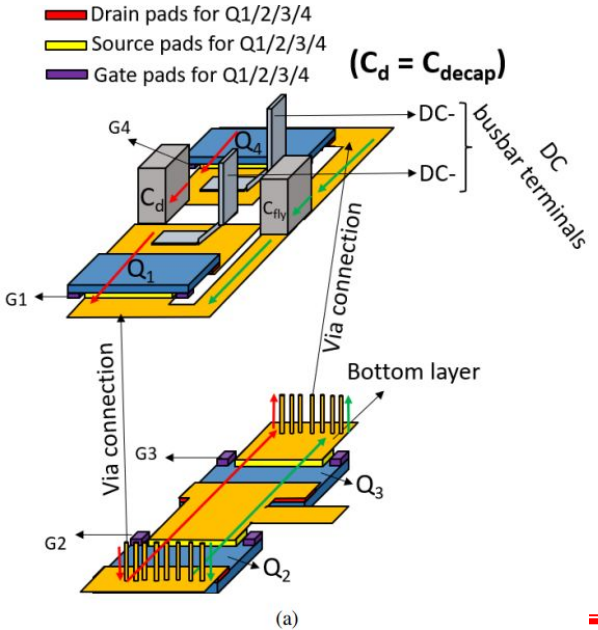
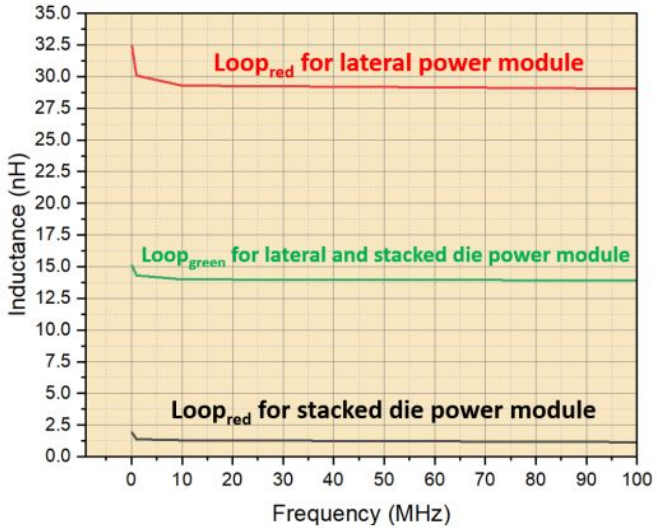
"Universal Stacked Die Layout Technique for Minimizing Parasitic Inductance in Flying-Cap Multilevel Converters"

A **universal** layout technique using 3D Stacked Die packages to **reduce power loop inductance up to 95%**, in Flying-Cap-Based multilevel (3,5,7,…) converters, significantly improving performance.







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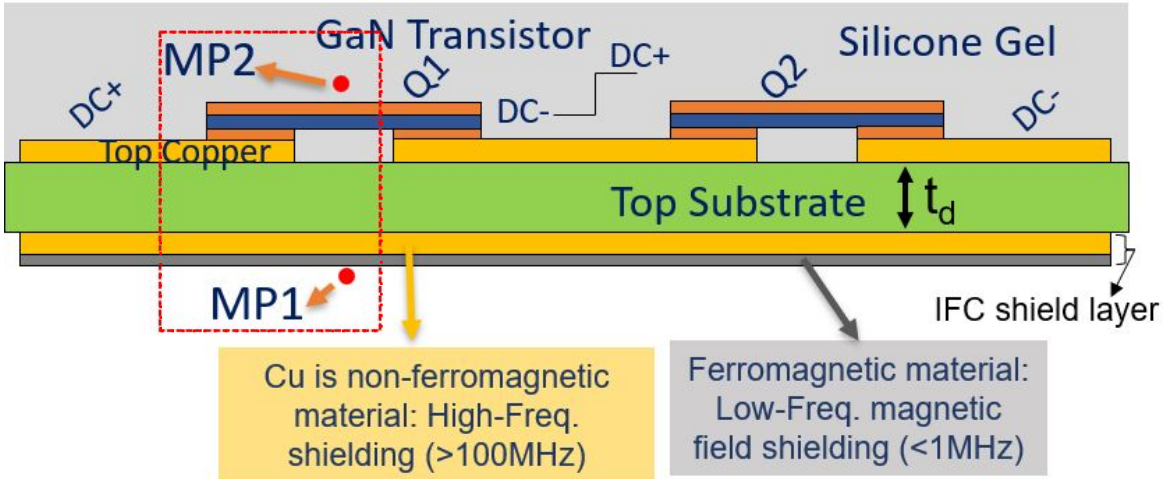
"Novel Integrated Ferromagnetic-Conductor (IFC) Multilayered Shield Layer for Parasitic Reduction in Power Modules"

A Power Module **Integrated *Ferromagnetic* Conductor (IFC)-based multilayer shields** is superior to traditional Cu conductor shields to effectively reduces parasitic loop inductance and provides better near-field emissions protection. A 0.3 oz Ni plated on Cu reduced L_{Loop} by 2%, 6.8%, and 4.3% for substrate dielectric thicknesses of 40, 120, and 300 µm, vs only Cu shield.

Near Field Emission Suppression



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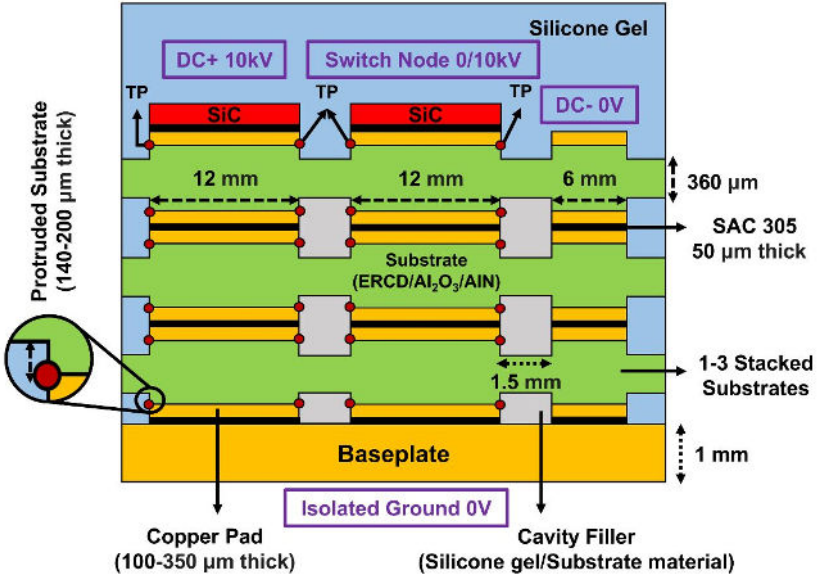
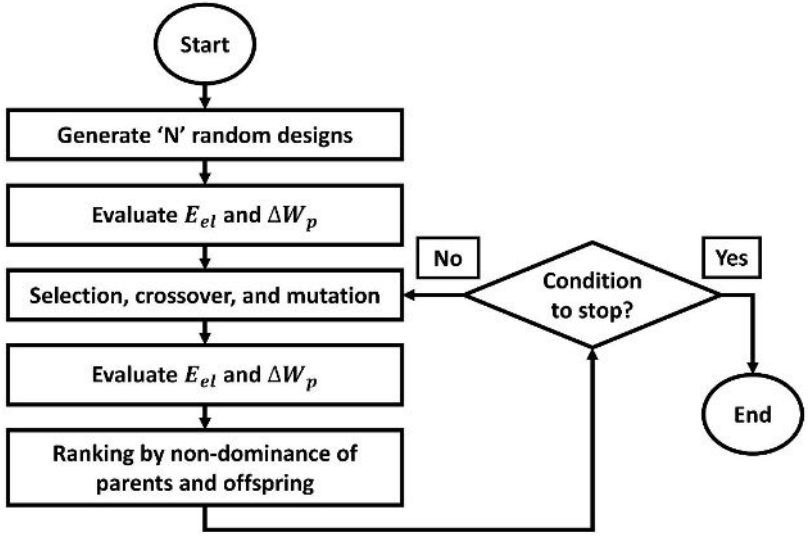
"AI-Based Optimization of Co-Designed Stacked Metallized Substrate Module Structures"

This technique **mitigates E-field intensities in stacked substrates to enhance the PD performance** of SiC power modules. A co-design framework incorporates electric and thermomechanical effects. A non-dominated sorting genetic algorithm (NSGA) explores trade-offs in PD mitigation and die-attach fatigue life under power cycling. **Optimization results indicate a 67.5% reduction in E- field intensity** vs conventional 10 kV designs.





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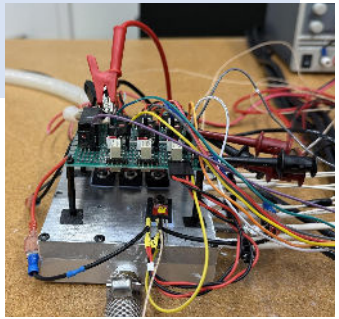
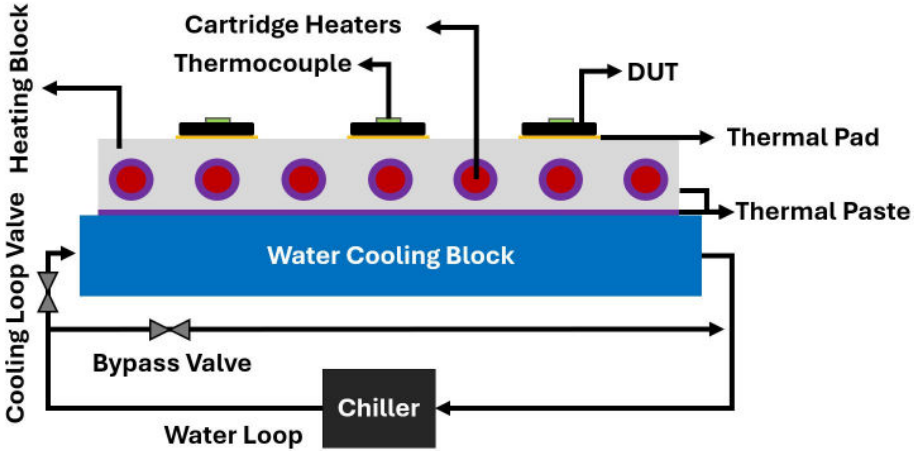
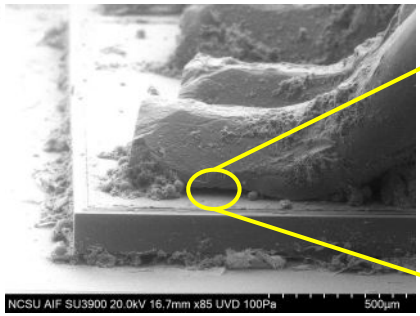
Package-Related Degradation Simulation in a SiC JFET/Si MOSFET Cascode under Power Cycling Test

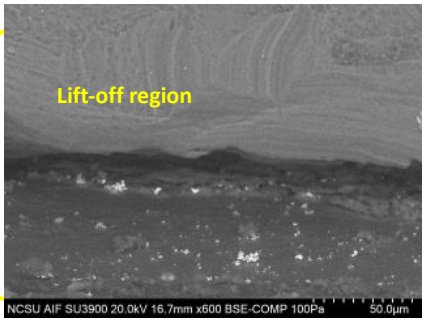
OBJECTIVE: Package-related degradation characterization of a SiC JFET/Si MOSFET cascode structure through:
1. Multiscale physics-based FEA models to capture component degradation and package-level stressors.
2. Performing a **Pseudo-power Cycling Test (PPCT)** to tune and validate the FEA models.
3. Develop Digital Twins for predicting Remaining Useful Life (RUL).

Pseudo-PCT setup









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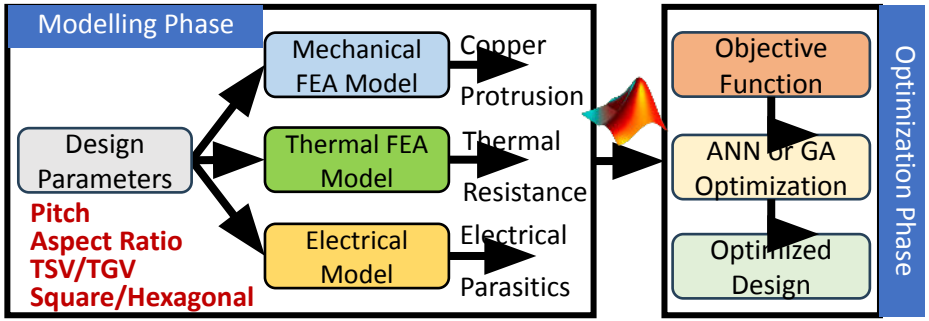
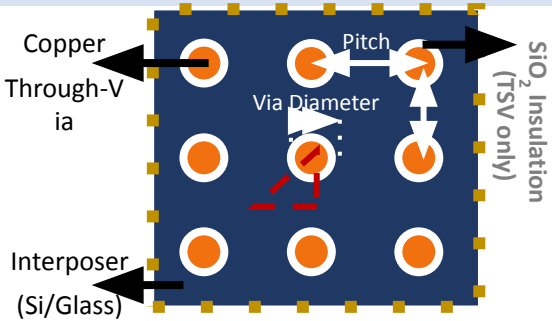
"Co-Design and ML-Based Optimization of Through-Via in Silicon and Glass Interposers for Electronic Packaging Applications,"

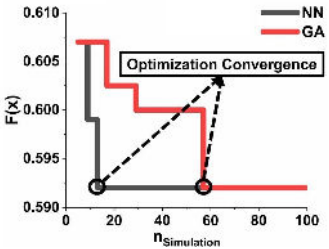
Investigates multiphysics effects of aspect ratio (AR) and pitch (P) in square and hexagonal Cu via arrays in Through Via Glass (TVG) & Si (TVS). Cu protrusion, thermal resistance, and electrical parasitics are optimized. An online artificial neural network (ANN) algorithm, as well as the conventional genetic algorithm (GA), are compared.

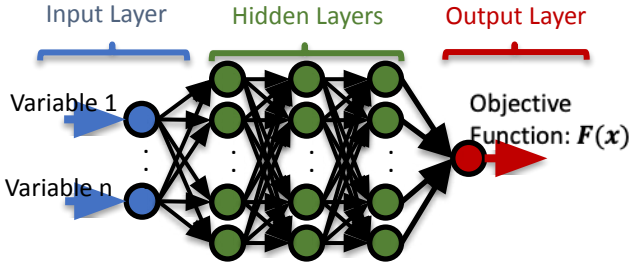
1. Developing a multi-objective optimization framework incorporating online artificial neural network (ANN).

2. Comparison of online ANN-based optimization and conventional Genetic algorithm (GA)









Digital Twin for Prognostics and Health Management

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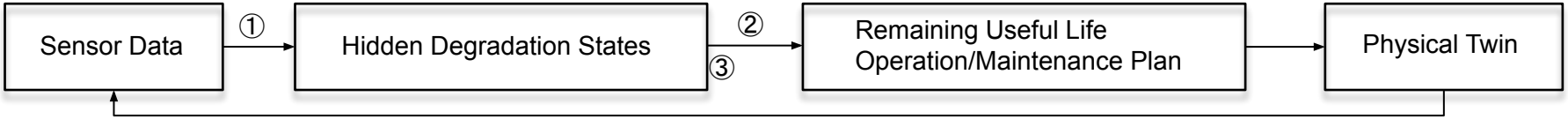
Impacts

- **EV:** PHM enables risk-aware, condition-based maintenance of EV power electronics, improving safety, reliability, and lifecycle cost efficiency.
- **Energy grid:** Early warning and uncertainty-aware failure prediction for grid assets, enhancing resilience, preventing cascading outages, and supporting reliable integration of renewable energy.



	Description	Model training	Data	Example
①			Multiphysics simulation	R_{DSon} vs. wire, solder cracking
②	UQ of Remanning Useful Life		Physics-of-failure, Experiment	Crack growth ~ (temperature, stress, dwelling time)
③			Physics-of-failure	Crack growth per cycle

Digital Twin for PHM of SiC Device

Prognostics and Health Management

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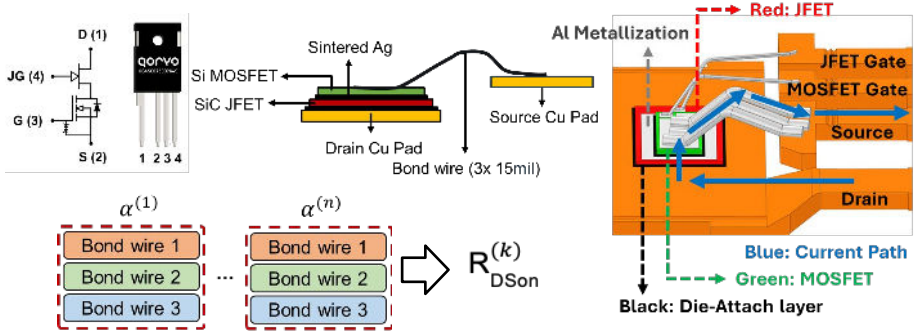
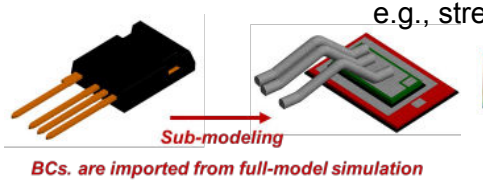
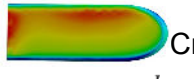
Observable and Hidden Data – COMSOL / Analytical



Degradation trajectory and Life – Mech. Sim., Experiment

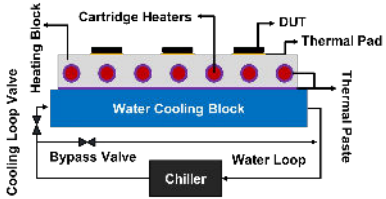
e.g., stress in bond-wire pad

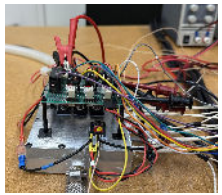


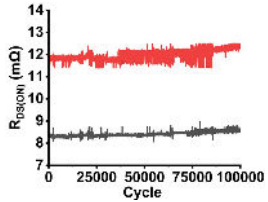


Crack growth model

$$\frac{d\alpha_i}{dN} = a\left(\Delta\varepsilon_{p,i}\right)^b, a, b: const.$$

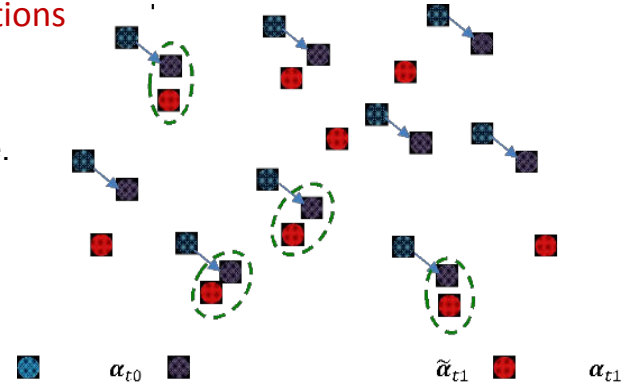




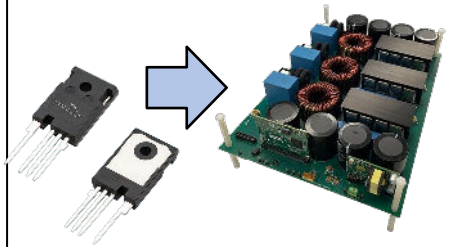


Filtering predictions

Accuracy increases every monitoring cycle.



Scalability and Extensibility **(Future Work)**



Failure physics

- Thermal stress (current)
- Insulation degradation
- Capacitor degradation
- Single-event hazard function

Research in Power Electronics & Packaging

"Semiconductor Electronics Mfgr Program – EPack-LAB"

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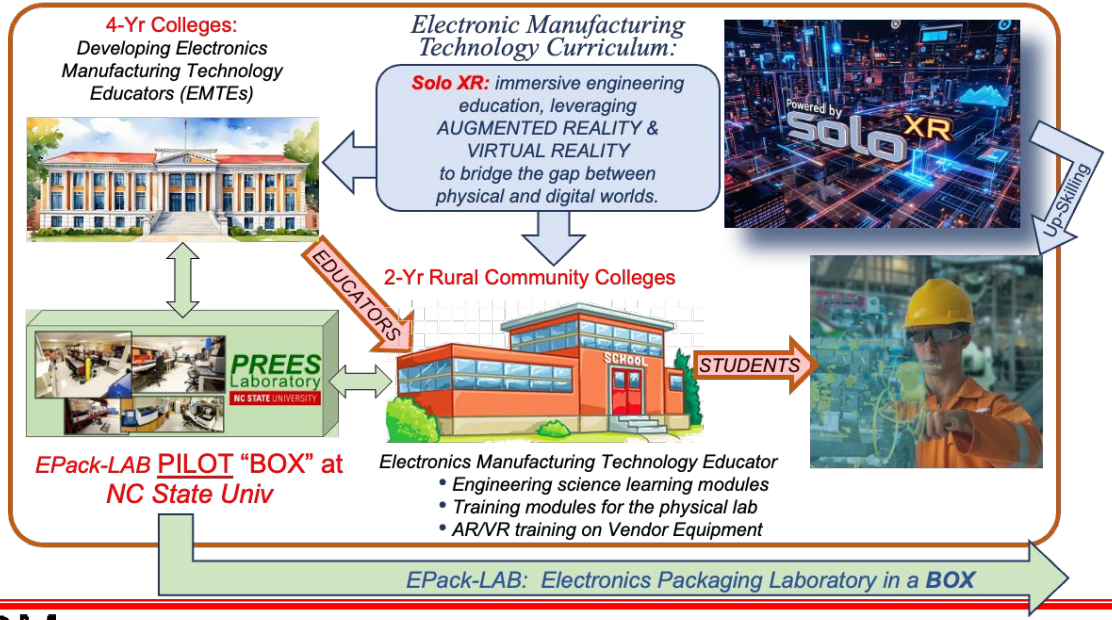
The "Electronic Packaging Lab in A Box" Program offers (1) curriculum for 2Yr & 4Yr schools to develop Community College Teachers, (2) a Deployable Hands-On Laboratory "BOX" (processing chips into products, and (3) leveraging AR/VR in a Master Trainer Multiplication Model to accelerate teacher development. Students use AR/VR for homework, projects and upskilling before and after they graduate.



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