Power Conversion Systems enabled by SiC-based Monolithic Bidirectional FET (BiDFET)

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Prof. Jay Baliga – SiC BiDFET device

Prof. Doug Hopkins – Advanced packaging of SiC BiDFET device

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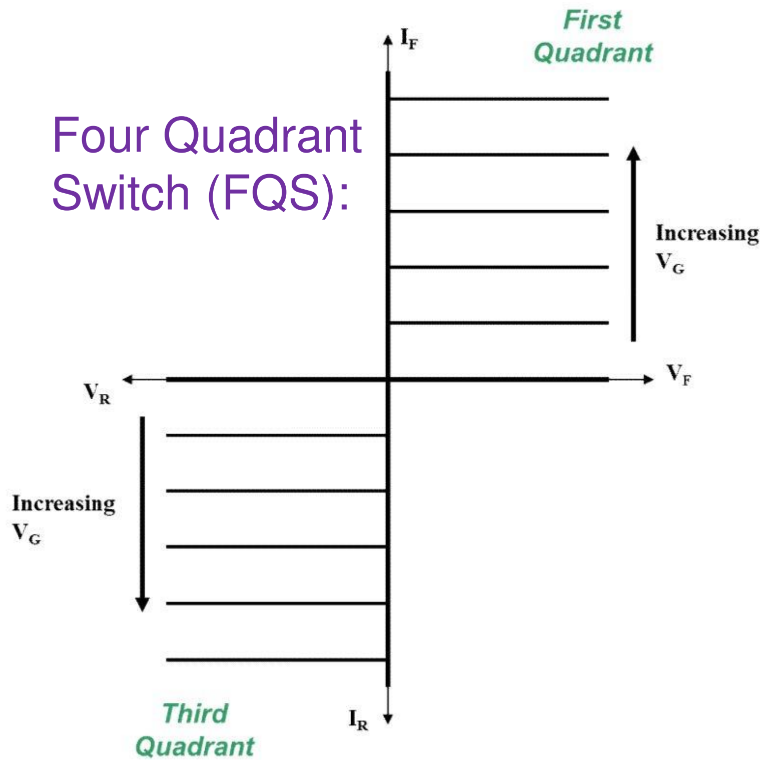
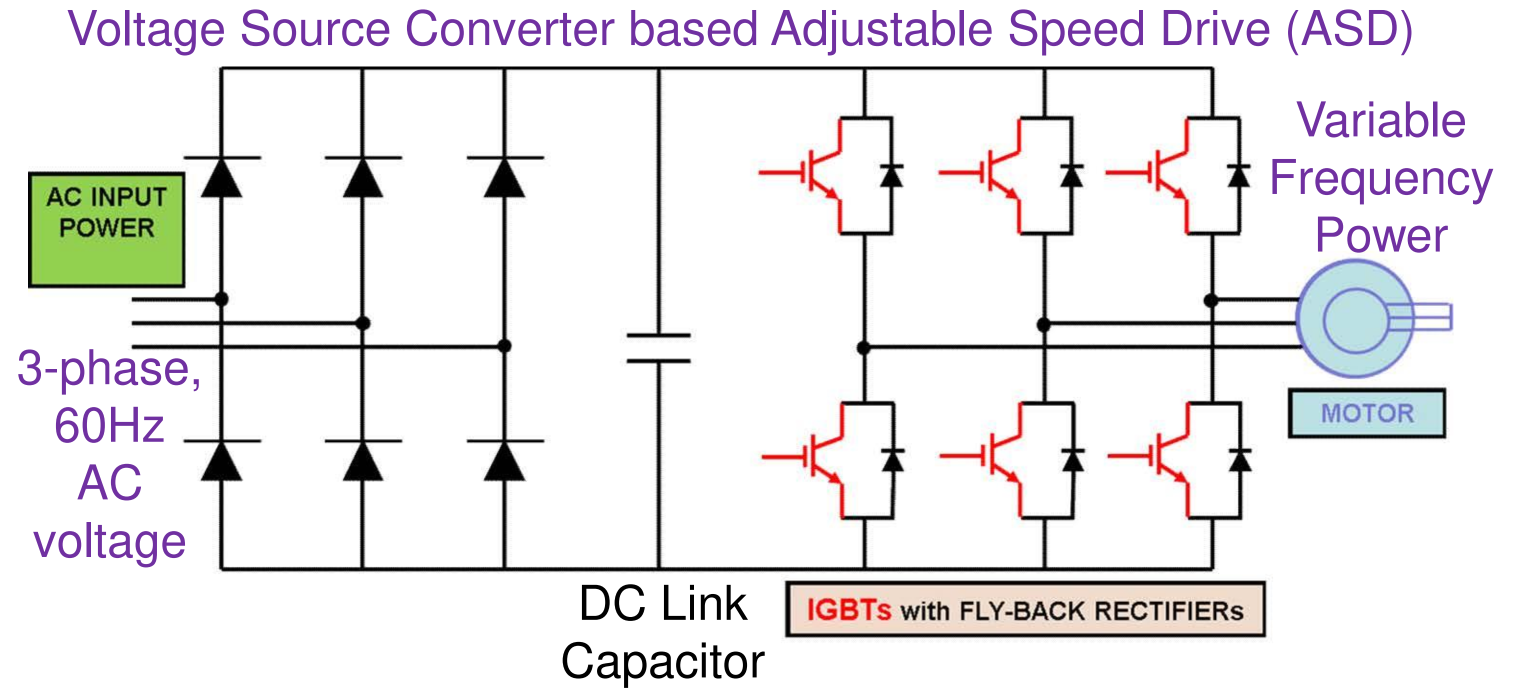
Four Quadrant Switch (FQS): The Ideal Power Device (The Holy Grail)

Four Quadrant Switch (FQS):



Voltage Source Converter based Adjustable Speed Drive (ASD)



Ideal Device Characteristics:

- Large Forward & Reverse Blocking Capability
- Bi-directional current flow
- Zero On-State Voltage Drop
- Fast Switching Capability
- Gate Voltage Controlled Output Characteristics
- Excellent Safe-Operating-Area

ASD needs Energy Storage Element:

- DC link capacitor as energy storage element
- Bulky
- Expensive
- Poor Reliability
- Degraded performance under high temperature
- Single point failure

B. J. Baliga, Fundamentals of Power Semiconductor Devices, 2nd Edition, Springer-Science, 2019
B. J. Baliga, "The IGBT Device", Elsevier, 2015

Four Quadrant Switch (FQS) Enabled Direct AC-AC Matrix or Cyclo Converter

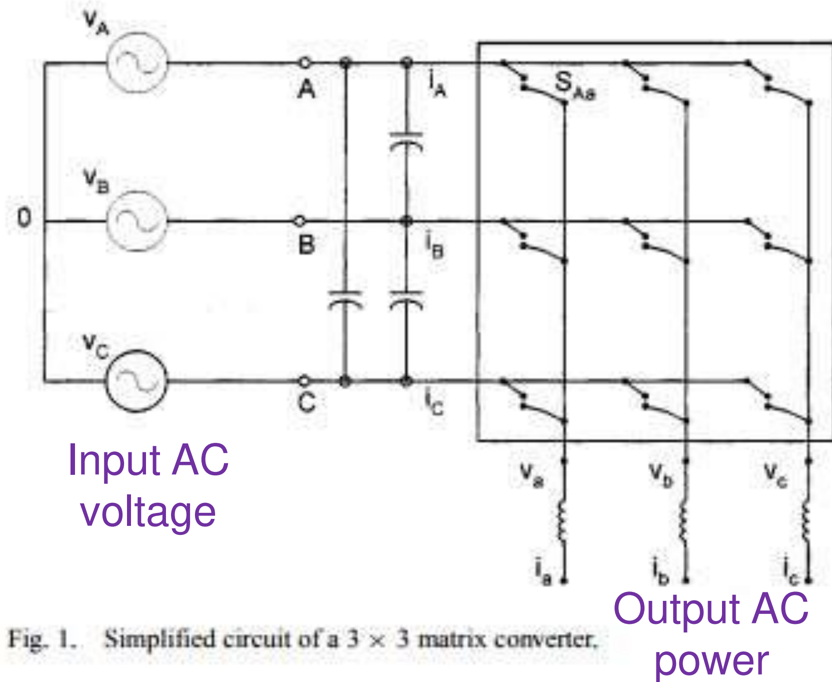


Fig. 1. Simplified circuit of a 3 × 3 matrix converter.

Input AC voltage

Output AC power

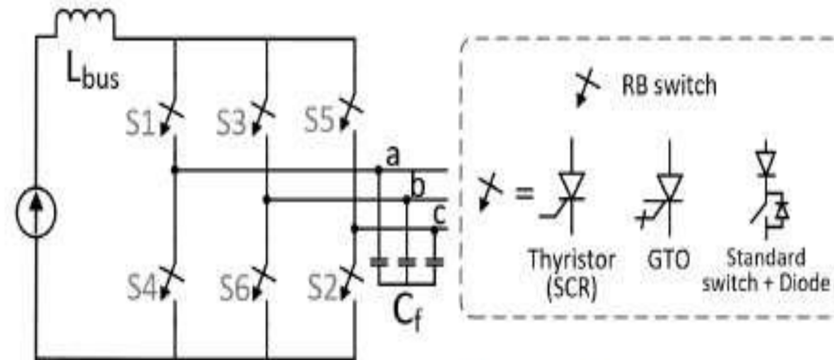
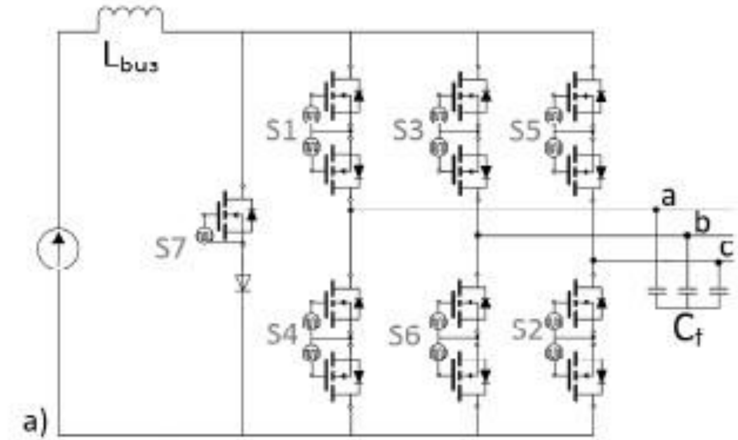


Fig. 1: Conventional CSI topology (H6-CSI) using reverse-voltage-blocking (RB) switches with regulated front-end dc-link current

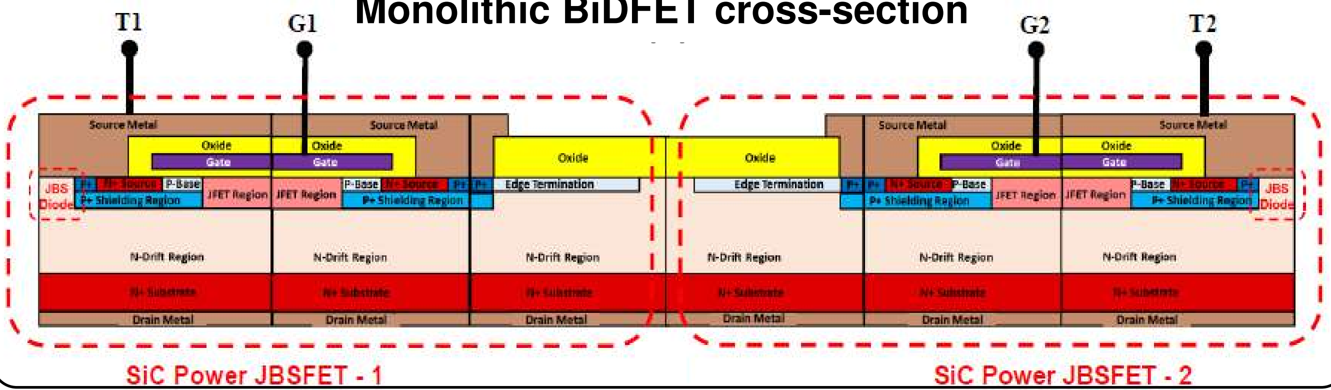


CSI with Bi-Directional [RB] Switches

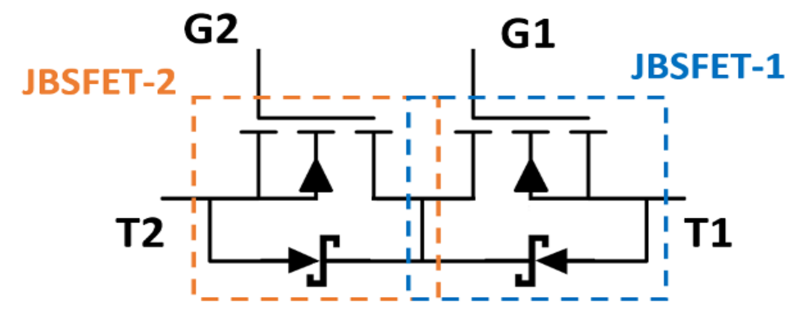
- Direct AC-AC Matrix or Cyclo Converter creates a variable output voltage with unrestricted frequency using an array of fully controlled four-quadrant bidirectional switches
- Does not need large energy storage element and DC-Link
- "Unfortunately, there were no such devices available" and "Consequently, multiple discrete devices had to be used to construct suitable switch cell" [P.W. Wheeler, et al, "Matrix Converters: A Technology Review", IEEE Trans. Industrial Electronics, vol. 49, no. 2, pp. 276–288, April 2002.]
- CSI have traditionally used Thyristor family reverse voltage blocking (RB) switches [eg. Thyristors, SGTO Thyristors, Symmetric IGCTs] – however, Thyristor family RB switches typically have low switching frequency
- WBG based SiC MOSFET with series connected SiC JBS [Junction Barrier Schottky] diode provides a RB switch with increased switching frequency for CSI – however, will have higher conduction voltage drop compared to single MOSFETs or IGBTs
- SiC BiDFET as a monolithic devices offers advantage of lower conduction voltage drop and higher switching frequency for CSI and Direct AC-AC Matrix or Cyclo Converter based power conversion systems

Monolithic SiC-based Bidirectional FET (BiDFET) Switch: 1200V, 20A DIE

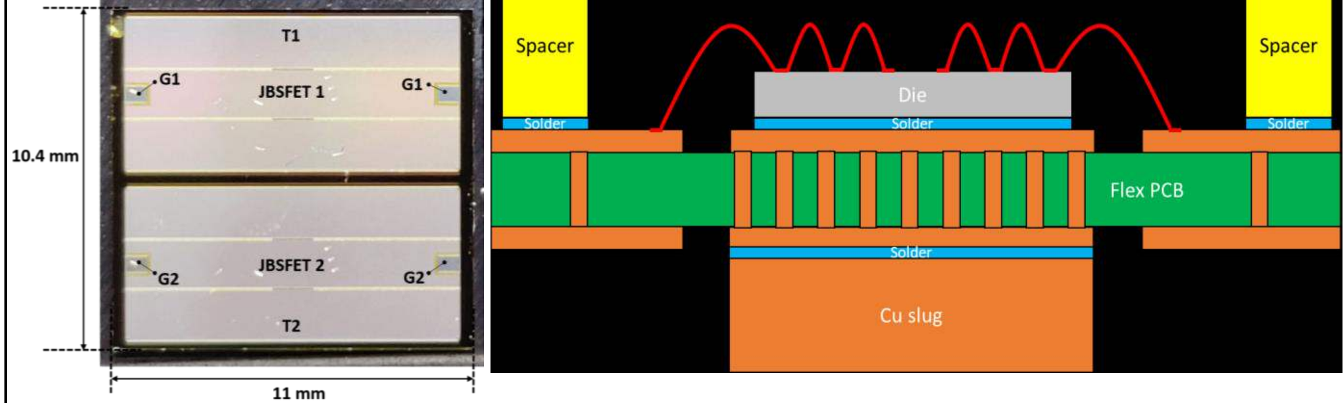
Monolithic BiDFET cross-section



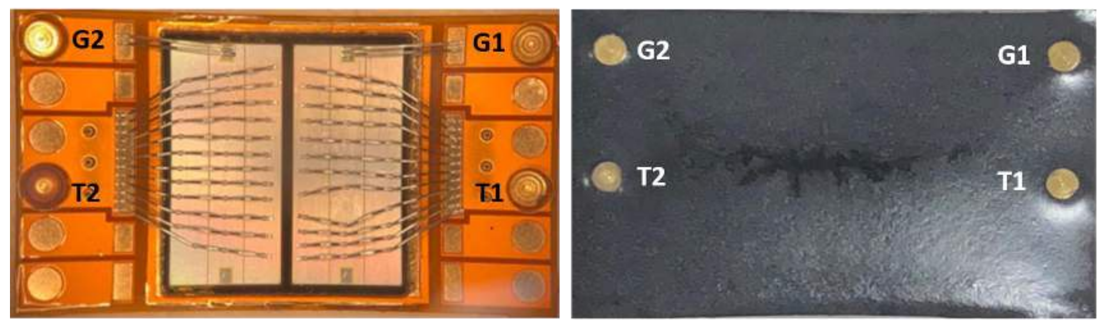
4-terminal Monolithic BiDFET circuit schematic



Fabricated BiDFET die:



Custom-made 4-terminal package for the BiDFET:



Comparison of fabricated 1.2 kV 20 A BiDFET with previous bidirectional switch implementations

Switch Configuration	Description	Number of components	On-State Voltage Drop (V)	Switching Loss
D1 D3 Q1 D2 D4	Diode Bridge + Asymmetric IGBT Neft & Schauder, IEEE Trans. Ind. Appl., vol. 28, pp. 546-551, 1992	5	8.6 [2 diodes + 1 IGBT]	High
Q1 Q2 D1 D2	Asymmetric IGBTs + Freewheeling diodes Moghe et al., ECCE, pp. 3848-3855, 2012	4	5.8 [1 diode + 1 IGBT]	High
Q1 D1 D2 Q2	Back-to-back symmetric IGBTs Takei et al., ISPSD, pp. 413-416, 2001	2	2.2 [1 symmetric IGBT]	Very High
Q1 Q2 D1 D2	SiC Power MOSFETs + JBS diodes Safari et al., IEEE Trans. Power Electron., vol. 29, no. 5, pp. 2584-2596, 2014	4	3.1 [1 diode + 1 MOSFET]	Low
Q1 D1 D2 D3 D4 Q2	Back-to-back SiC Power MOSFETs + antiparallel and series JBS diodes Ahmed et al., IEEE Trans. Power Electron., vol. 32, pp. 1232-1244, 2017	6	3.1 [1 diode + 1 MOSFET]	Low
	Four-terminal SiC Monolithic BiDFET	1	1.0 [1 BiDFET]	Low

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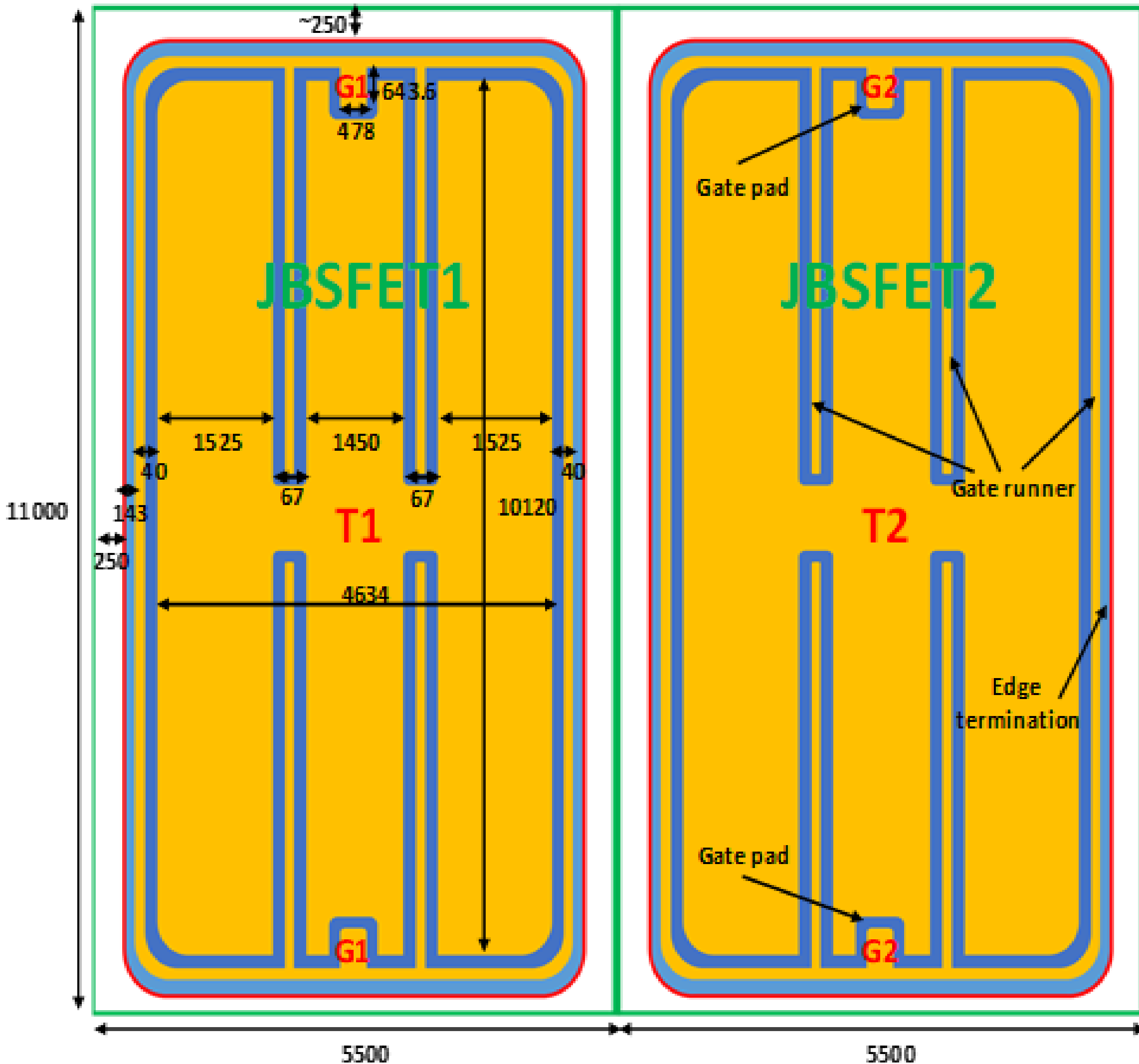
Gen-1 SiC BiDFET: Chip Design



Objective 1:
- Rated Blocking Voltage = 1.2 kV
- Breakdown Voltage > 1.4 kV
- Use Hybrid JTE Edge Termination BV > 1.6 kV

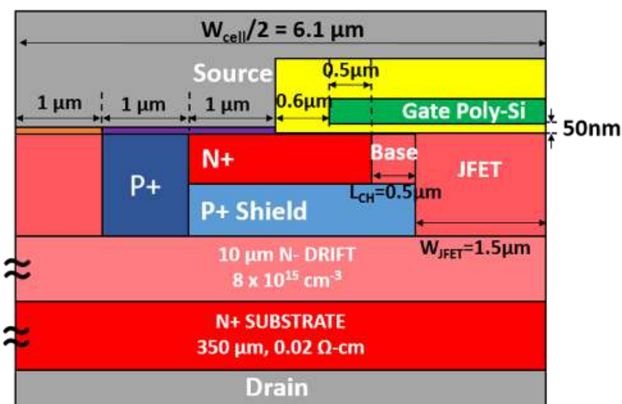
Objective 2:
- On-Resistance of BiDFET = 50 mΩ
- Each JBSFET On-Resistance = 25 mΩ
- Use JBSFET Active Area = 0.45 cm2

Objective 3:
- Low Internal Gate Resistance < 1 Ω
- Use Gate Runners

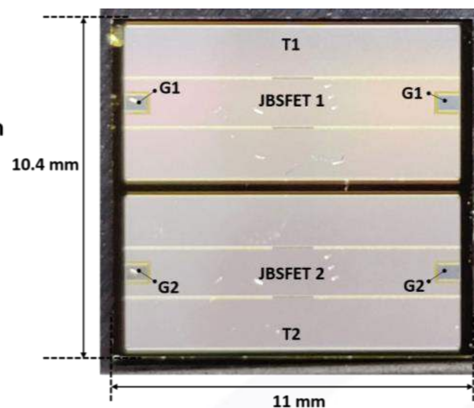
Objective 4:
- Improved Packaging and Board Interconnect
- Use Two Gate Bonding Pads per JBSFET

SiC BiDFET Gen-1: Single Chip

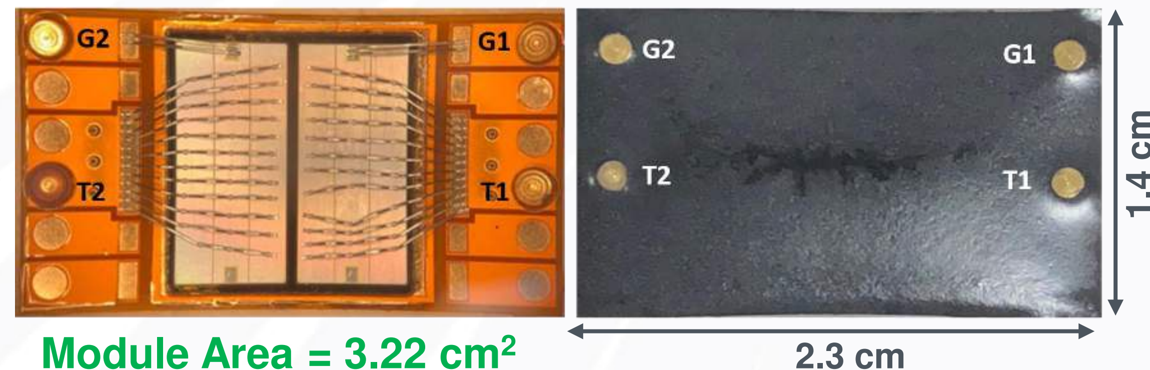
Internal JBSFET cross-section



Fabricated BiDFET die



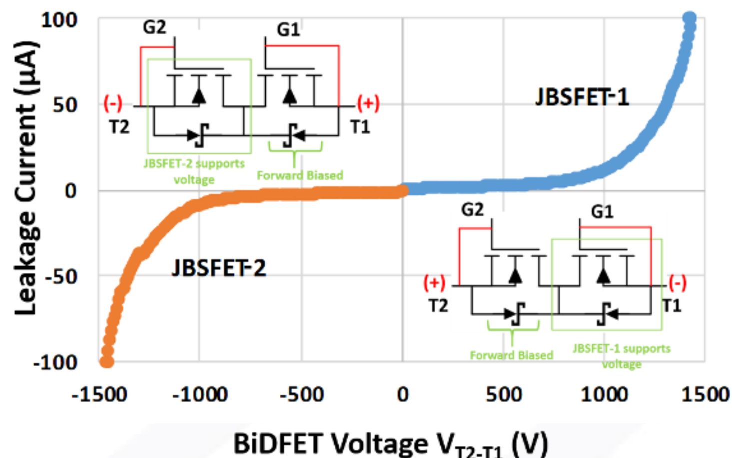
Custom-designed 4-terminal package for the BiDFET



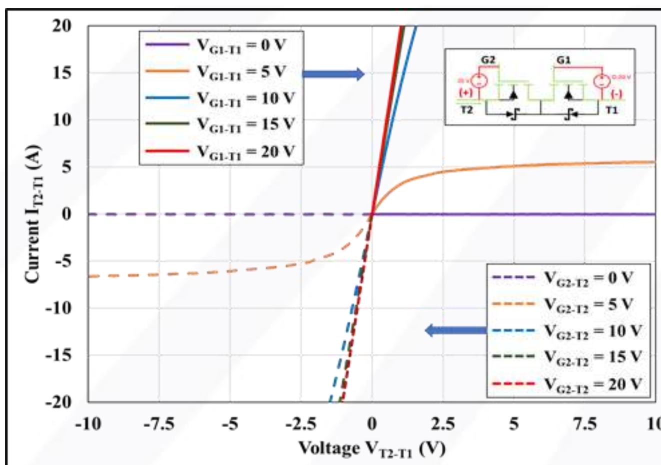
Module Area = 3.22 cm^2

2.3 cm

BiDFET blocking characteristics



BiDFET output characteristics

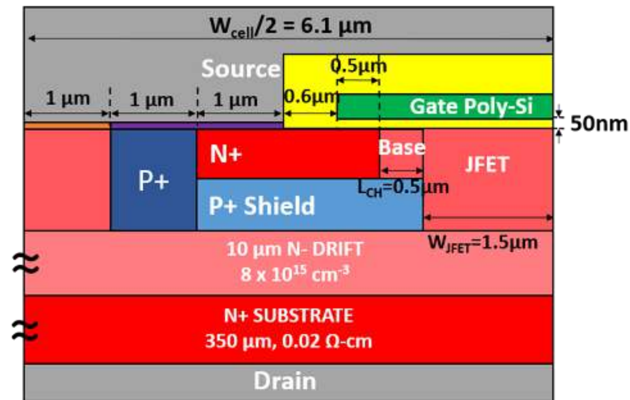


- Blocking Voltage > 1400 V
- On-Resistance = 50 mΩ
- First Pass Success
- Used to demonstrate 1ϕ 2.3 kW converter
- C_{iss} = 11,000 pF
- C_{oss} = 500 pF at 1000 V
- C_{rss} = 50 pF at 1000 V

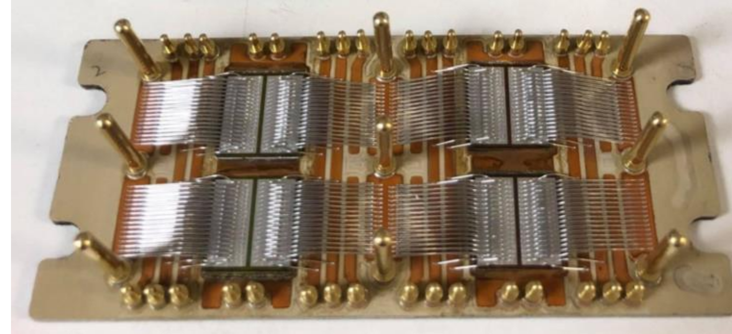
SiC BiDFET Gen-1: Parallel Chips

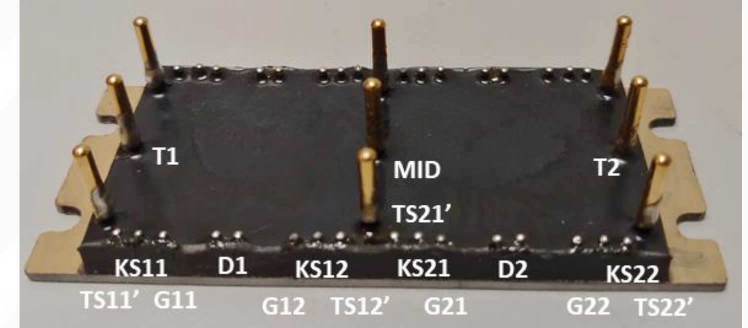
Objective: Demonstrate Reduced On-Resistance BiDFET by Paralleling Two Chips for 3ϕ Converter Application

Internal JBSFET cross-section



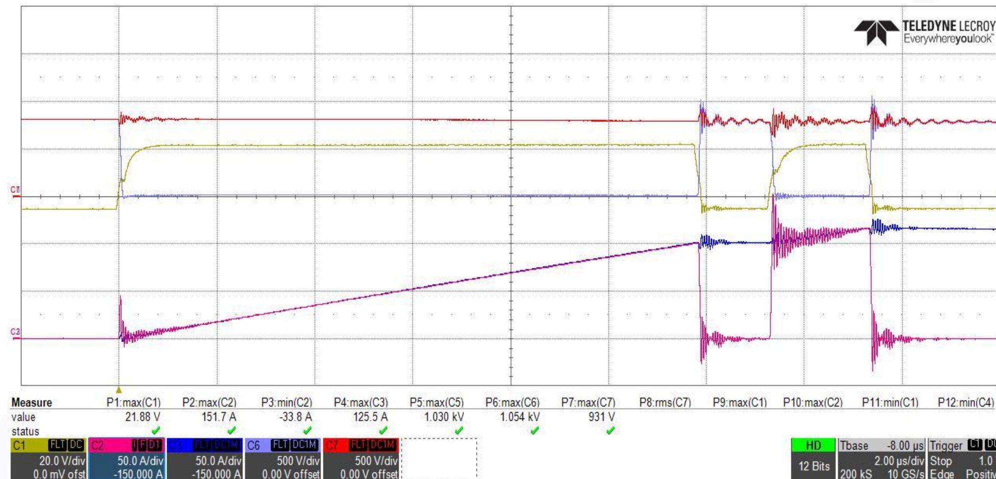
Custom-designed Half-Bridge Module with Paralleled BiDFET chips





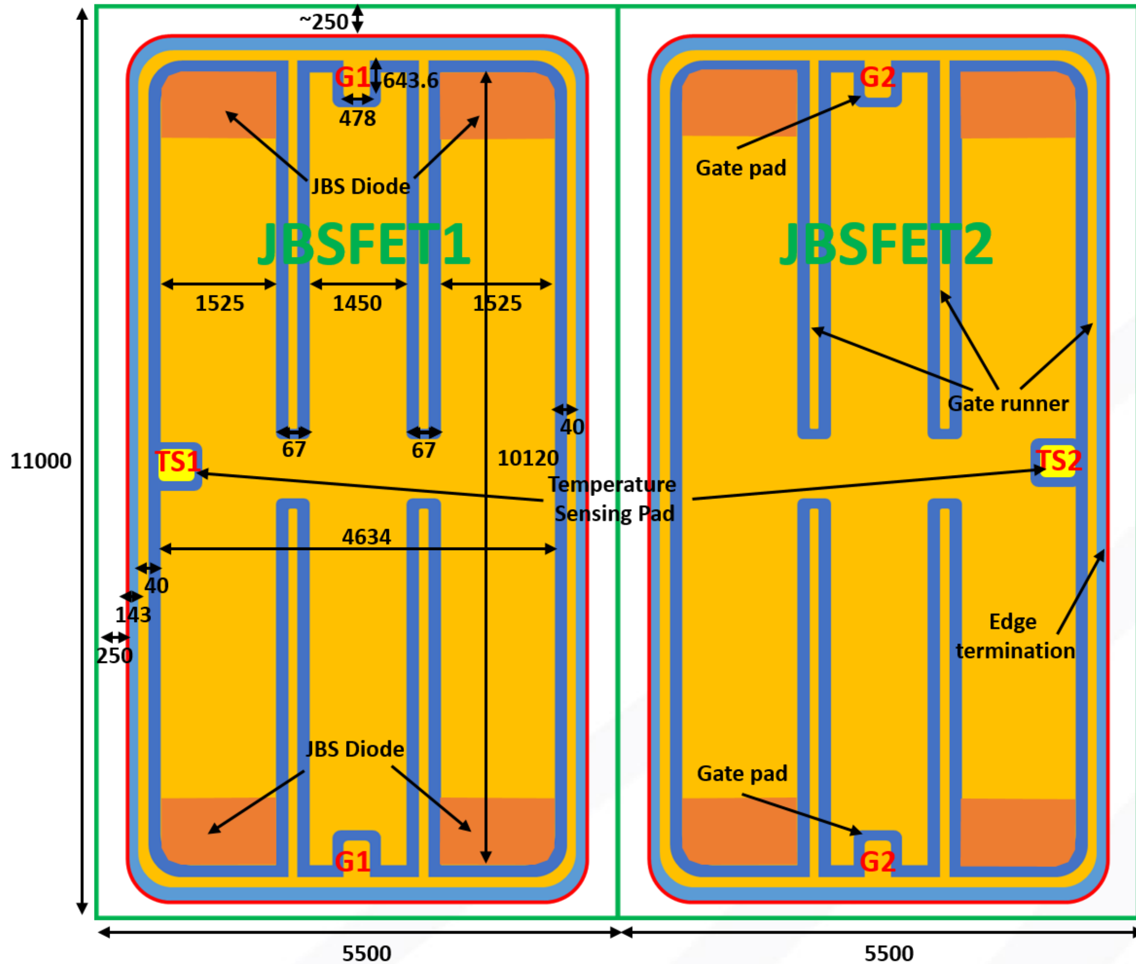
Module Area = 27 cm^2

BiDFET DPT Switching Waveforms



- Turn-on and Turn-off like a single Gen-1 BiDFET chip
- Switching Losses (800 V, 20 A):
  - E_{ON} = 1350 μJ
  - E_{OFF} = 460 μJ
  - E_{TOTAL} = 1810 μJ

Gen-2 BiDFET: Achieve 2x Lower R_{on}



Objective:
- Rated Blocking Voltage = 1.2 kV
- Breakdown Voltage > 1.4 kV
- Device On-Resistance = 25 mΩ

Conventional Doubling Die Size Approach:
- Very Low Yield
- Die Size exceeds X-Fab Maximum Reticle Size
- Impossible

Parallel Gen-1 Dies:
- Achieved in Modules

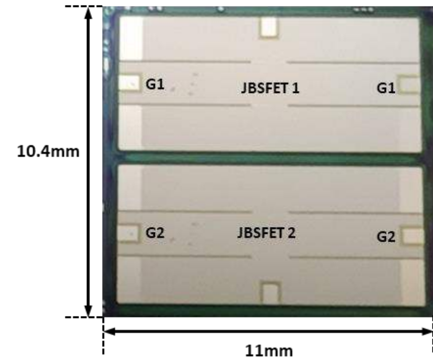
New Design and Process Strategy Created:
- Separate JBS Diode from MOSFET Cells
- Reduces Cell Pitch to 2.8 μm from 6.1 μm
- Reduces Specific On-Resistance to 5.3 mΩ-cm^2
- Ascribe 10 % Active Area to JBS Diode
- R_{on} = 26 mΩ achievable

Additional Objective:
- Add Integrated Temperature Sensor
- Use Poly-Silicon Gate Electrode Resistance
- No additional processing required

SiC BiDFET Gen-2 Single Chip

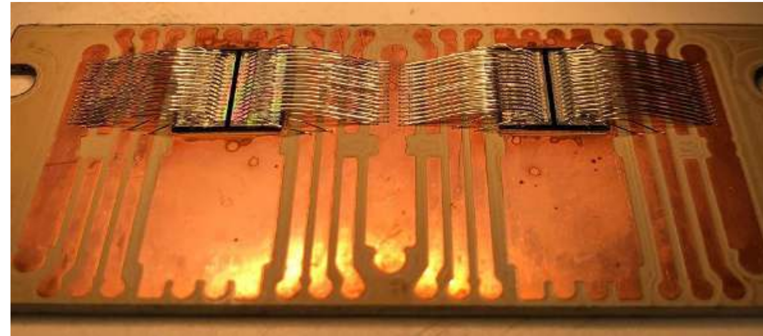
Objective: Demonstrate Reduced On-Resistance BiDFET with Single Chip for 3ϕ Converter Application

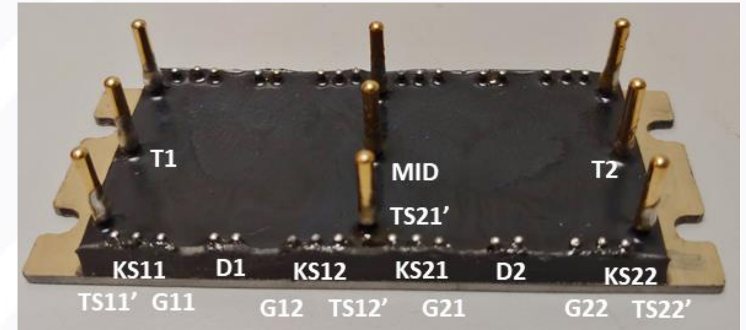
Gen 2 BiDFET Chip



Die Size: 10.4 mm x 11 mm

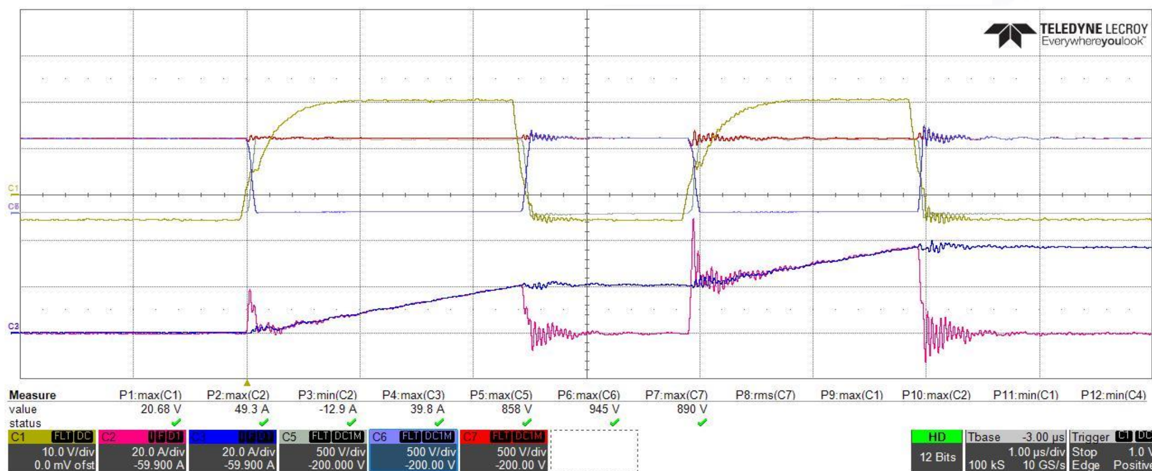
Custom-designed Half-Bridge Module with Single Gen-2 BiDFET Chip





Module Area = 13.5 cm^2

BiDFET DPT Switching Waveforms



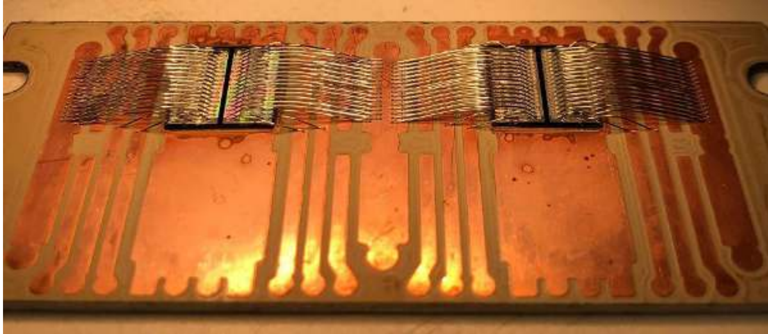
- Turn-on and Turn-off like a single Gen-1 BiDFET chip
- Switching Losses (800 V, 20 A):
  - E_{ON} = 1120 μJ
  - E_{OFF} = 250 μJ
  - E_{TOTAL} = 1370 μJ

Single Gen-2 BiDFET chip can handle 20 A (V_{ON} = 0.5 V).

SiC BiDFET Single Gen-2 Chip vs BP-1 Two Gen-1 Chips in Parallel

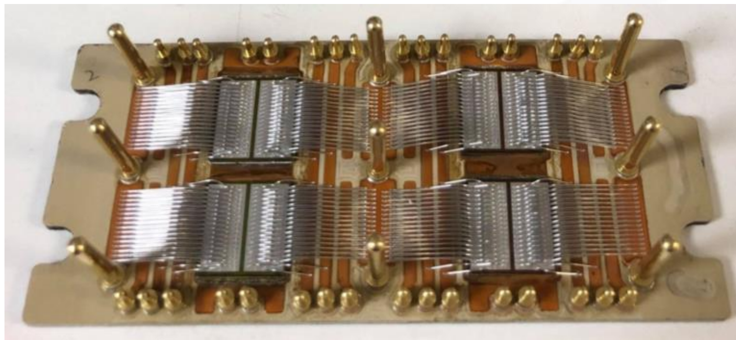
Objective: Demonstrate Reduced On-Resistance BiDFET with Single Chip for 3ϕ Converter Application

Module with Single Gen-2 BiDFETs



Area = 13.7 cm²

Module with Two Gen-1 BiDFETs in Parallel

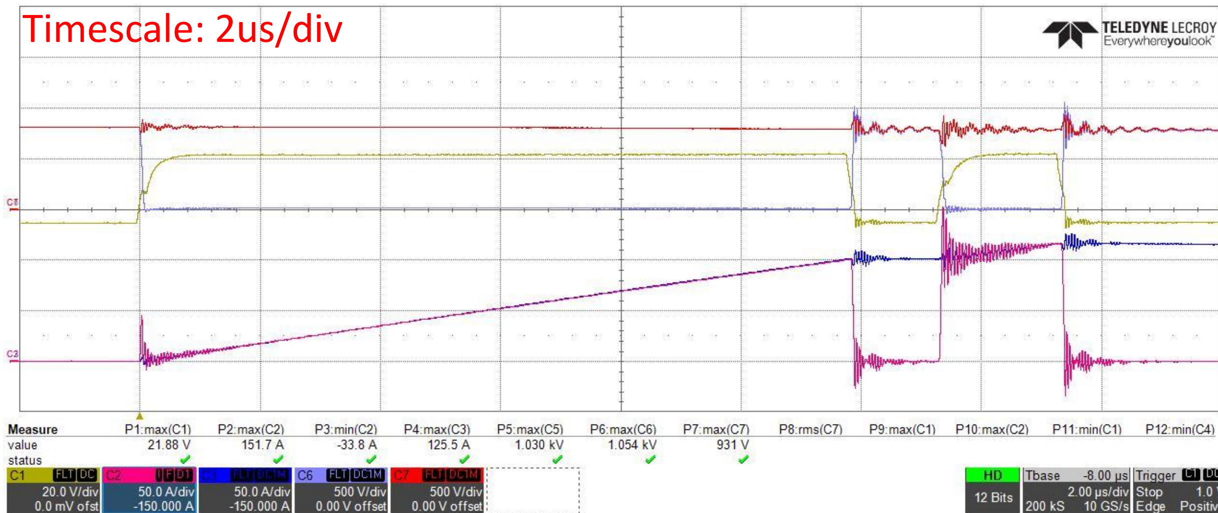


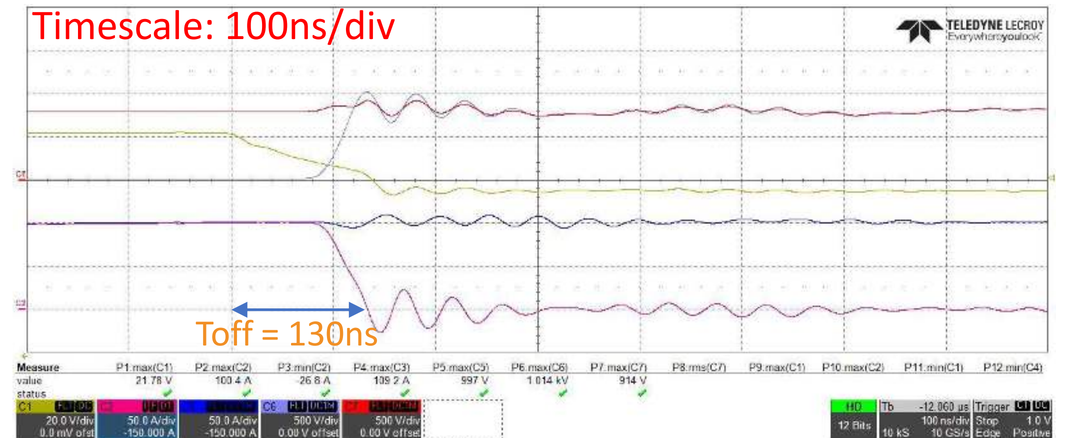
Area = 27.4 cm²

Parameter, Units	Gen 1 (2 Chips)	Gen 2 (1 Chip)	Improvement
Chip Area, cm^2	2.28	1.14	2x
$R_{DS,ON}$, mΩ	25	27	-
g_M, S	15	15	-
C_{ISS}, pF	15100	11730	1.3x
C_{OSS}, pF	1050	600	1.75x
C_{RSS}, pF	70	70	-
E_{ON}, µJ	1350	1120	1.2x
E_{OFF}, µJ	460	250	1.8x
E_{TOTAL}, µJ	1810	1370	1.3x

BiDFET characterization

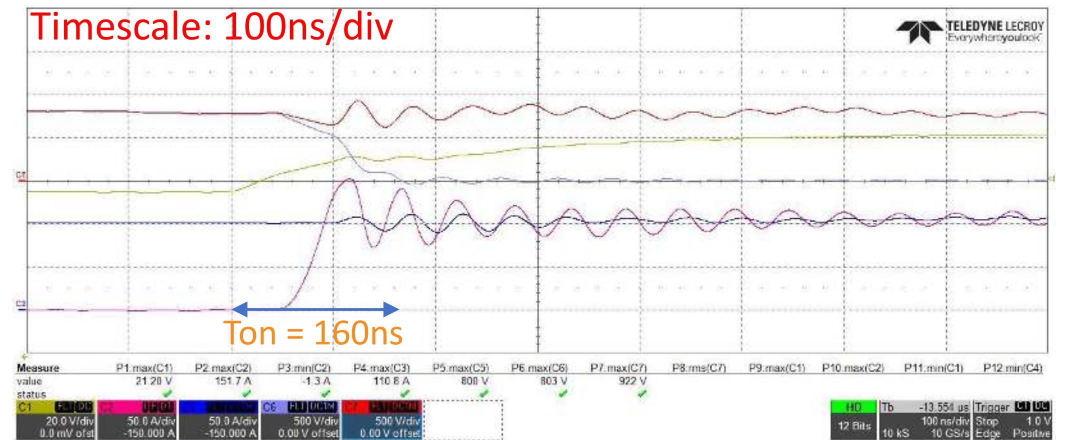
DPT results of BiDFET module with two Gen-1 dies in parallel at 800V, 100A.





Turn-OFF transition

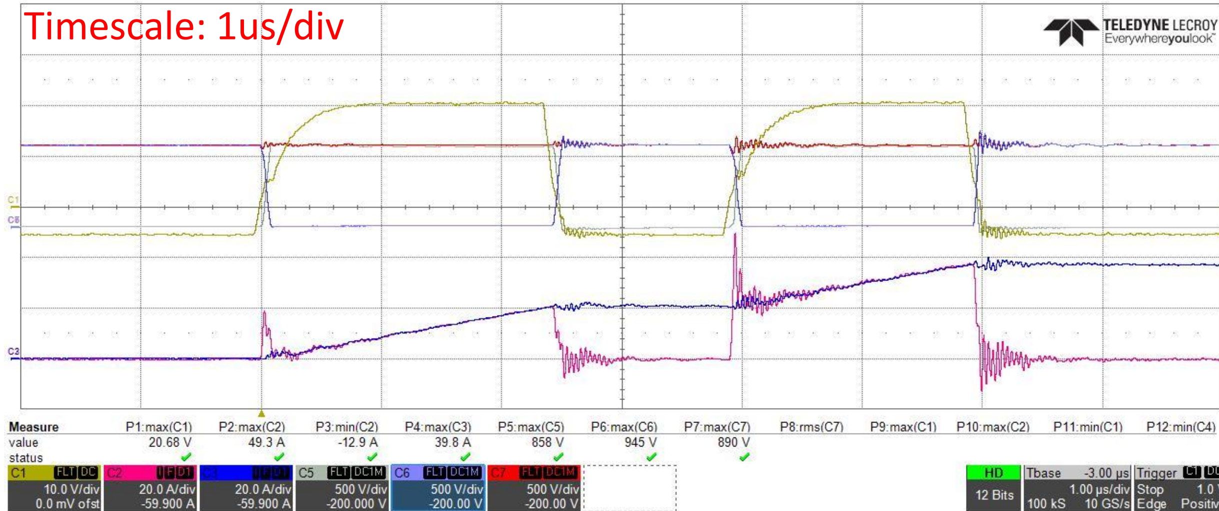
Channel 1: Gate-source voltage (20 V/div)
Channel 2: DUT current (50 A/div)
Channel 3: Inductor current (50 A/div)
Channel 6: DUT voltage (500 V/div)
Channel 7: DC bus voltage (500 V/div)

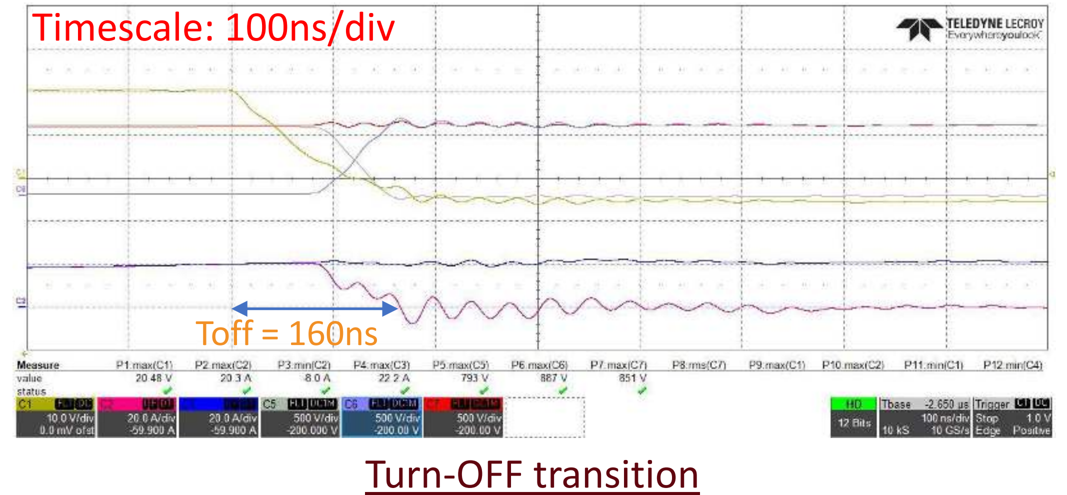


Turn-ON transition

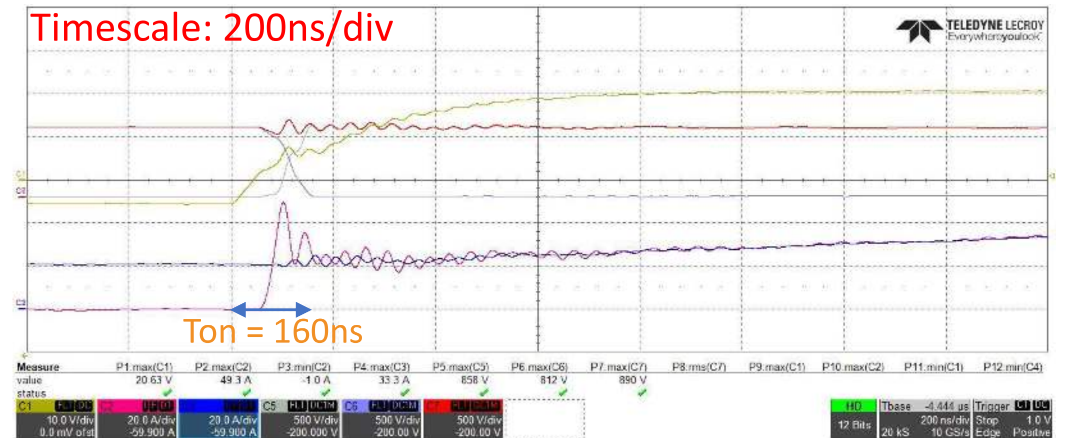
BiDFET characterization

DPT results of BiDFET module with Gen-2 dies at 800V, 20A.





Turn-OFF transition



Turn-ON transition

Channel 1: Gate-source voltage (10 V/div)
Channel 2: DUT current (20 A/div)
Channel 3: Inductor current (20 A/div)
Channel 5: Freewheeling device voltage (500 V/div)
Channel 6: DUT voltage (500 V/div)
Channel 7: DC bus voltage (500 V/div)

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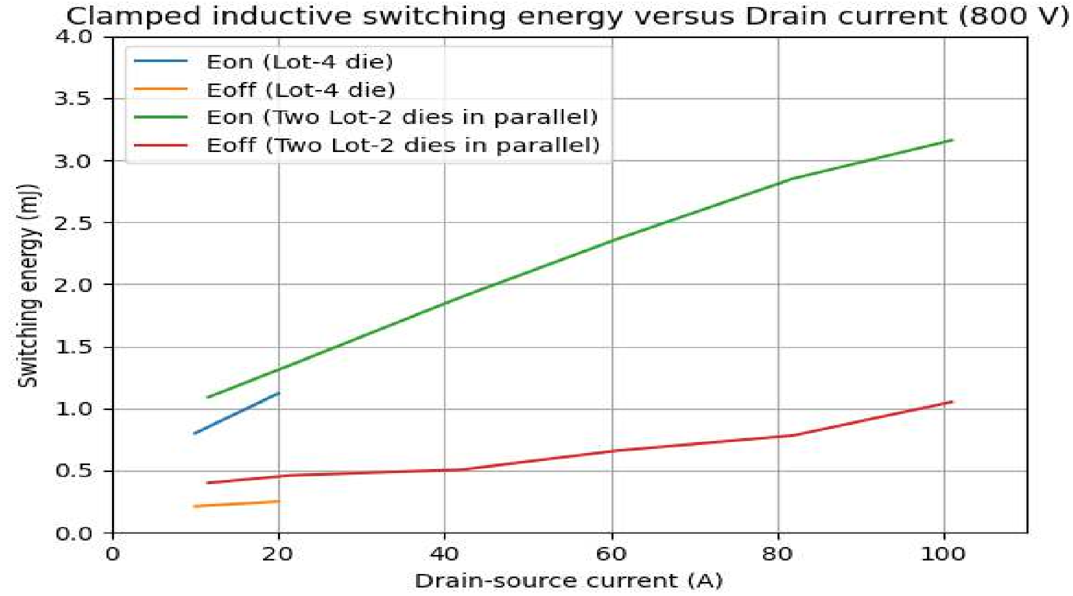
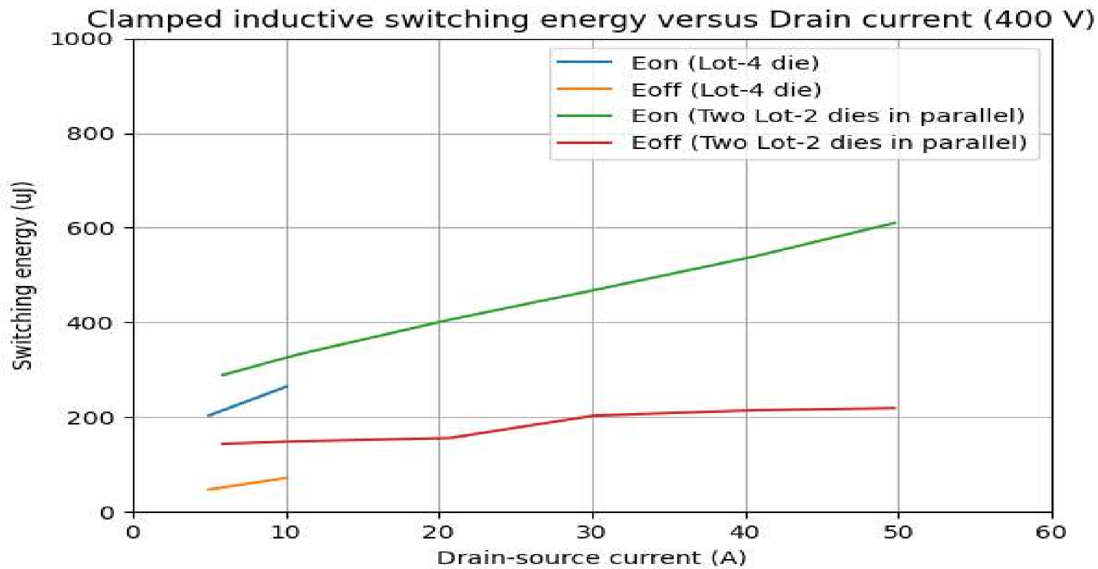
BiDFET characterization

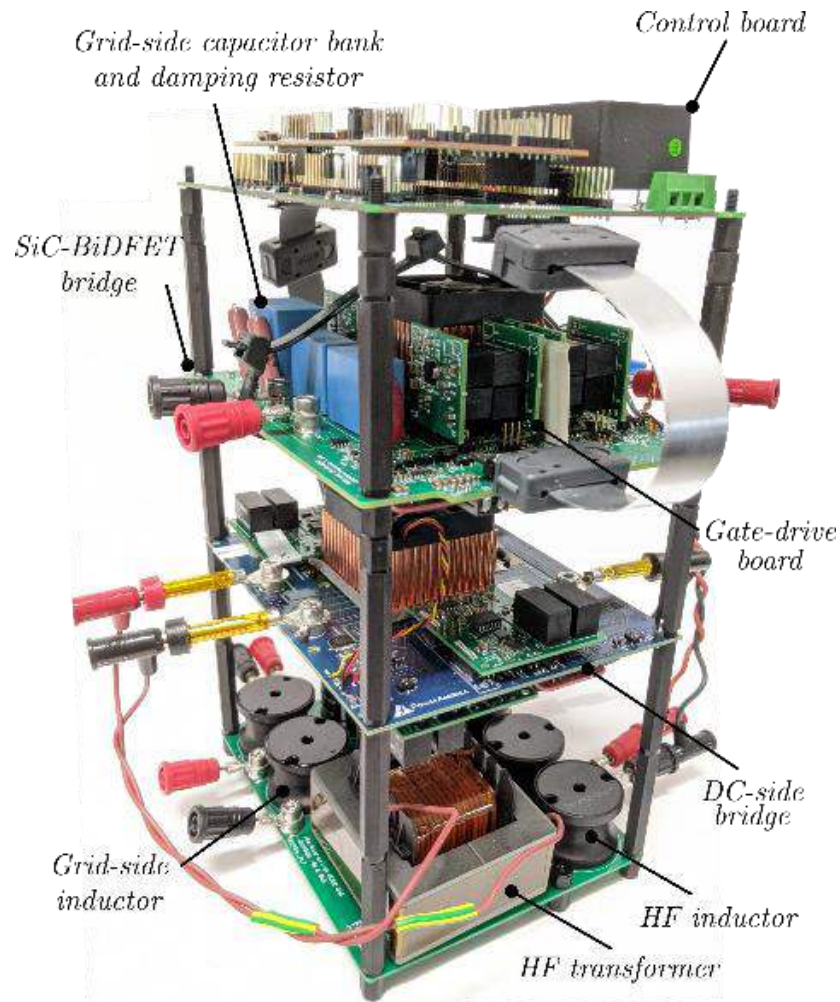




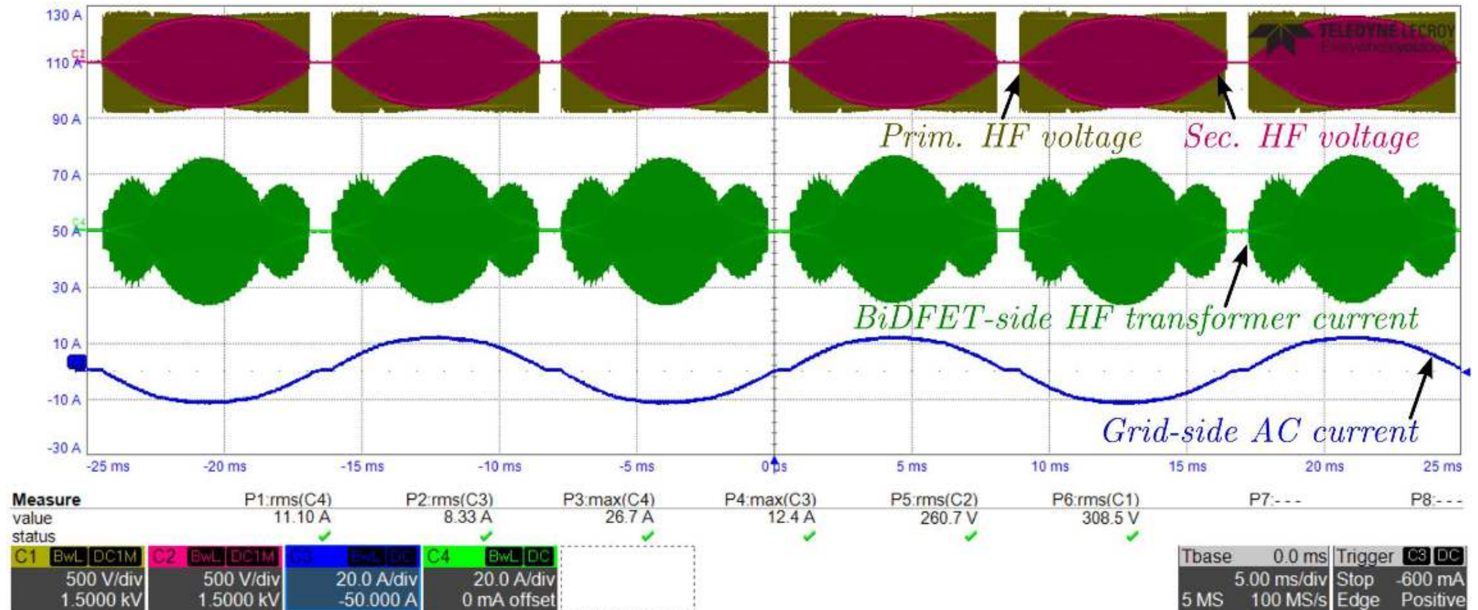
BiDFET	Vds (V)	Ids (A)	Eon (mJ)	Eoff (uJ)	Esw (mJ)
Two Gen-1 dies in parallel ($R_{g,on}$ = 3.3Ω, $R_{g,off}$ = 1Ω)	800	11.6	1.09	399.78	1.49
		21.5	1.35	460.58	1.81
		42.1	1.90	507.20	2.41
		60.8	2.36	660.30	3.02
		81.9	2.85	781.20	3.63
		101.0	3.16	1051.50	4.21
	400	5.9	0.29	143.58	0.43
		10.8	0.33	149.00	0.48
		20.7	0.41	156.05	0.57
		30.1	0.47	203.14	0.67
		40.7	0.54	214.60	0.75
		49.7	0.61	219.05	0.83
Gen-2 die ($R_{g,on}$ = 7.5Ω, $R_{g,off}$ = 2Ω)	800	10.0	0.80	211.00	1.01
		20.0	1.12	249.67	1.37
	400	5.0	0.20	47.00	0.25
		10.0	0.26	71.71	0.33

Dynamic characterization of BiDFET modules at 400V and 800V operation.

2.3 kW, 1-ph grid connected converter prototype enabled by 1200V, 20A SiC BiDFET



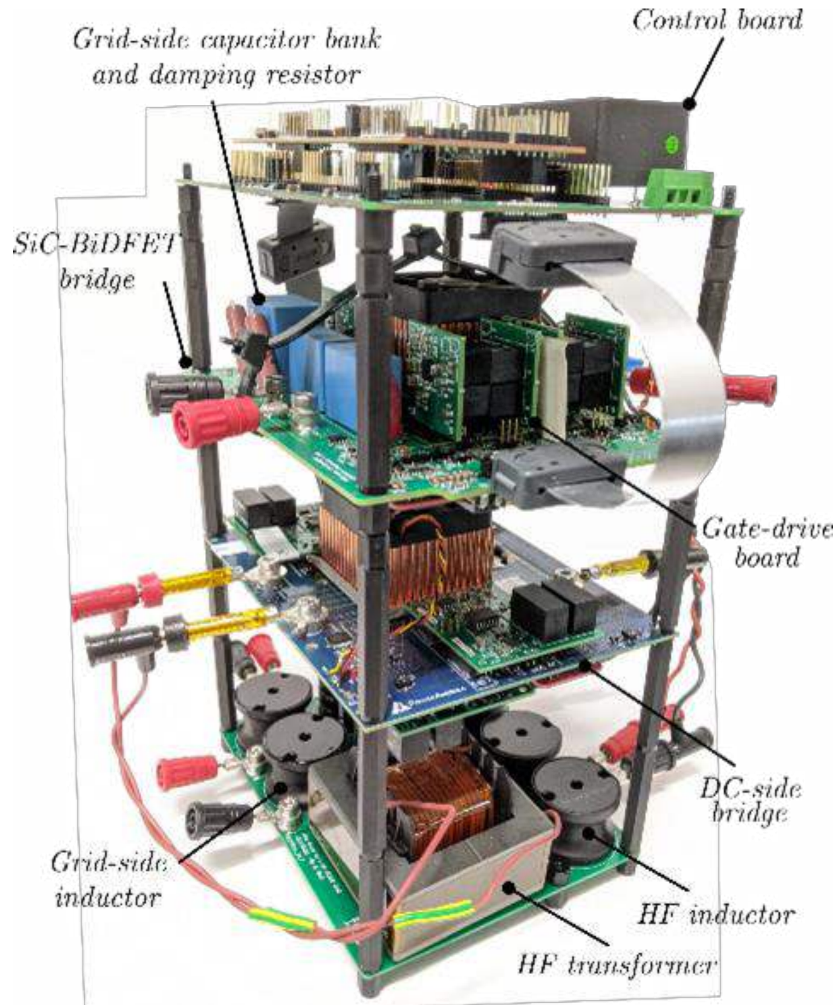
Hardware prototype of the AC/DC DAB converter for 400 V DC input and 120V/240V/277V AC output.



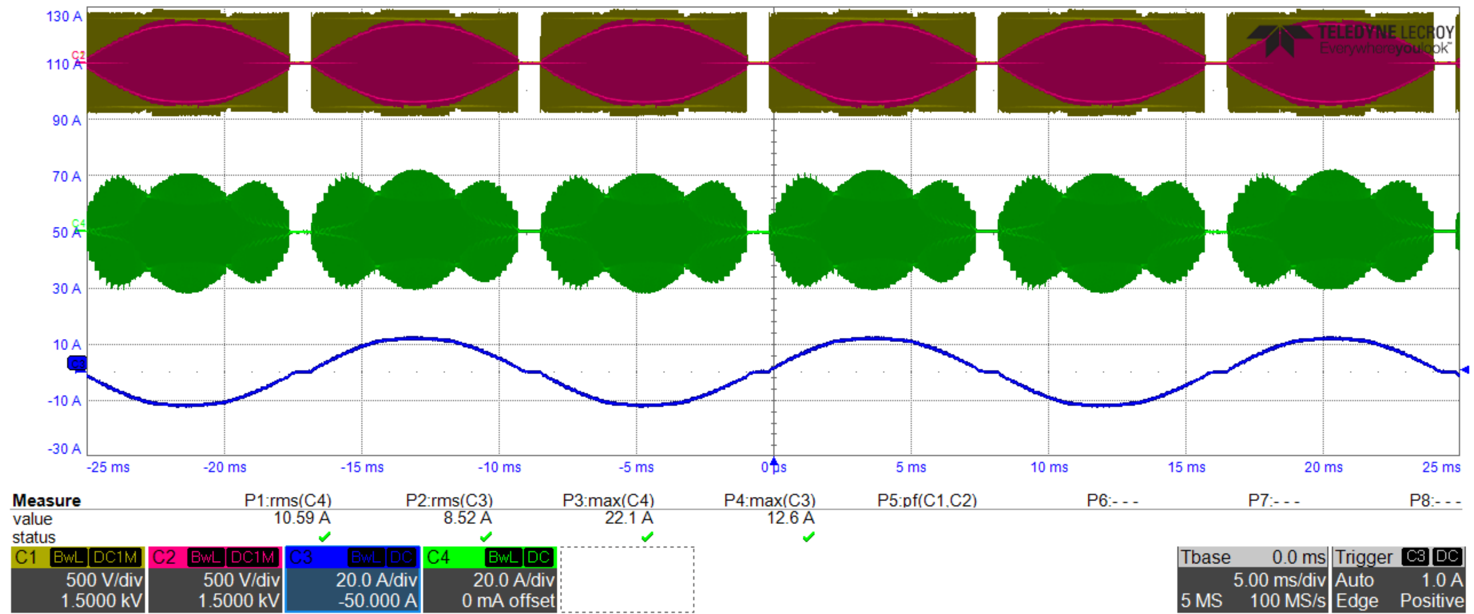
High frequency transformer voltages/current and grid side current at 100% load at 277 V AC voltage.

- Full load operation at 400 V input, 277 V RMS AC output at 2.3 kW power.
- Total harmonic distortion in grid-side current: 4.7%
- Power factor: 0.9998

2.1 kW, 1-ph grid connected converter prototype enabled by 1200V, 20A SiC BiDFET



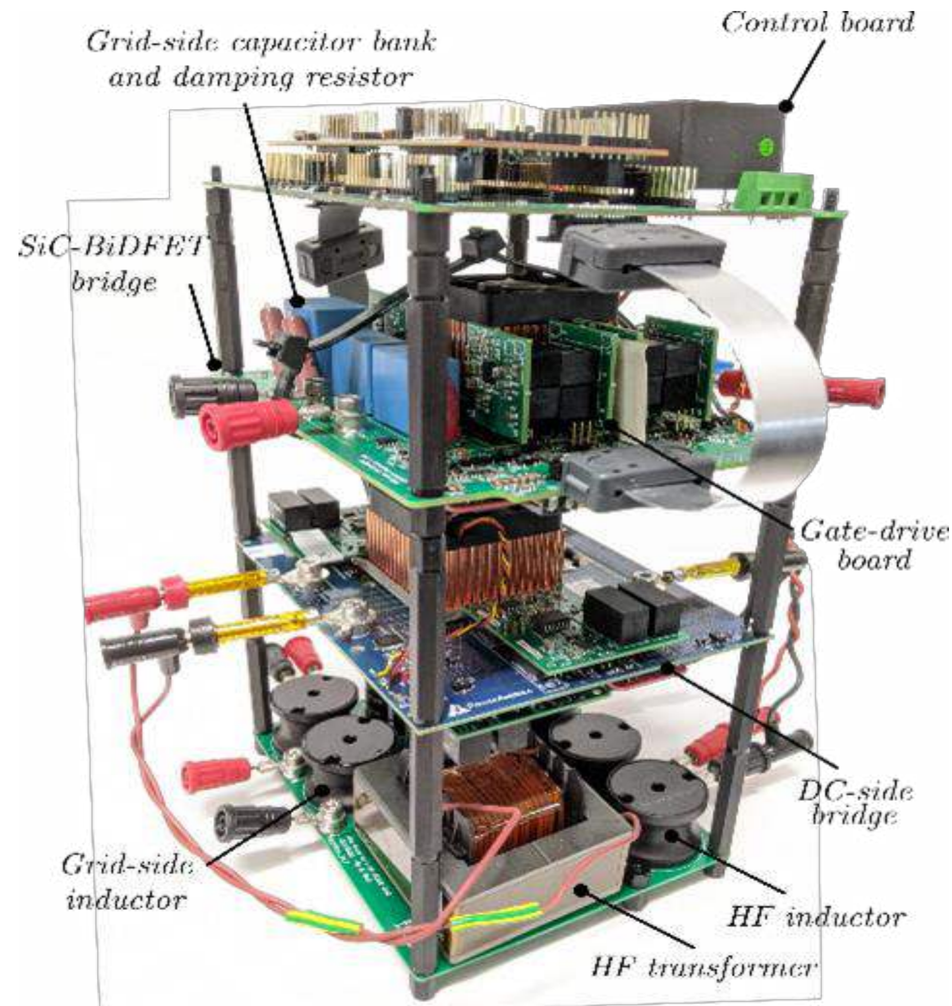
Hardware prototype of the AC/DC DAB converter



High frequency transformer voltages/current and grid side current at 100% load at 240 V AC voltage.

- Full load operation at 400V input, 240V RMS output at 2.1 kW
- Total harmonic distortion in grid-side current: 4.8%
- Power factor: 0.9998

2.1 kW, 1-ph grid connected converter prototype enabled by 1200V, 20A SiC BiDFET



Hardware prototype of the AC/DC DAB converter

2021-07-20 12:10:53 CH 6 1P2W Sync: U6 LPF: OFF Manu 600 V Manu 10 A Upper: 2MHz Lower: 0.1 Hz 50ms HOLD

U_{rms6}	246.530 V	S_6	2.11670 kVA
I_{rms6}	8.5860 A	Q_6	−0.03891 kvar
P_6	2.11634 kW	ϕ_6	− 1.053 °
λ_6	−0.99983	f_6	59.9978 Hz

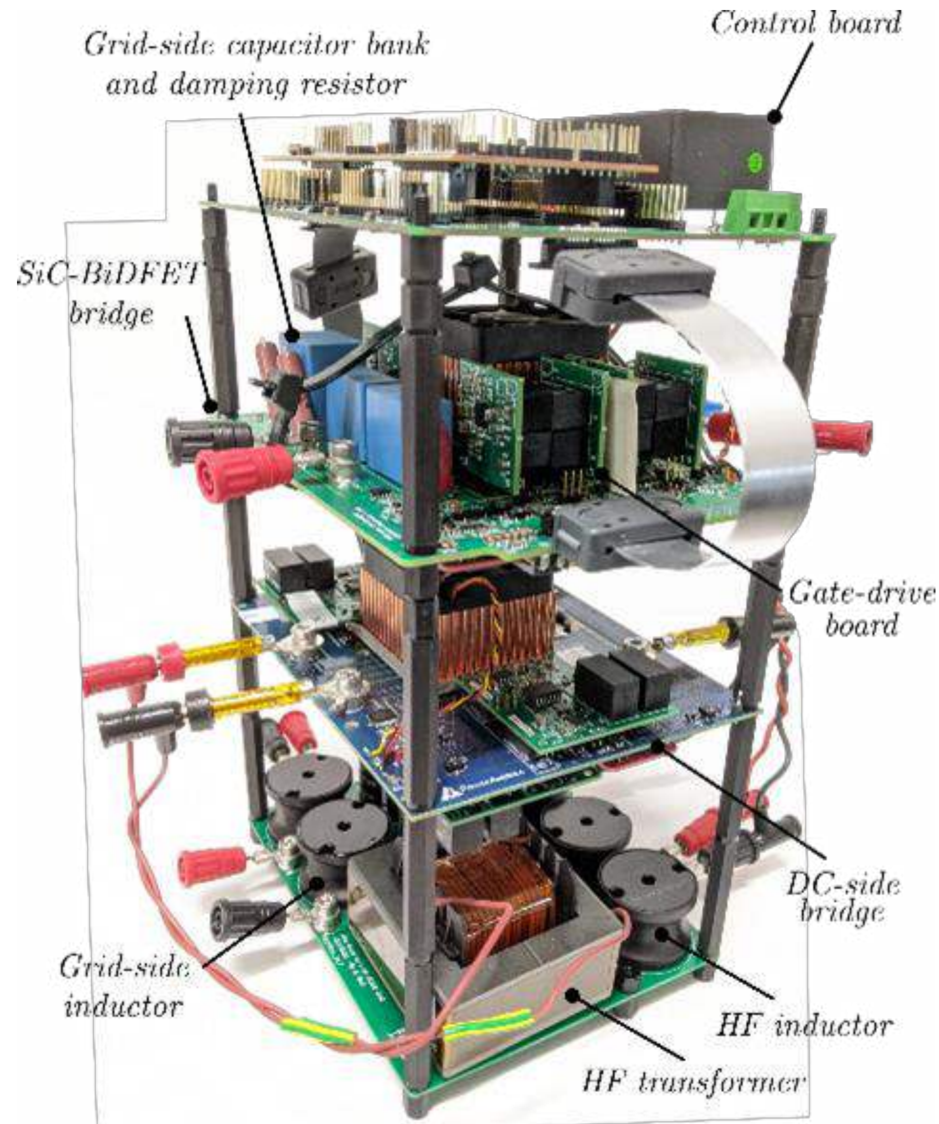
2021-07-20 12:10:58 CH 6 1P2W Sync: U6 LPF: OFF Manu 600 V Manu 10 A Upper: 2MHz Lower: 0.1 Hz 50ms HOLD

I_{rms6}	8.5860 A	I_{pk6+}	12.8538 A
I_{mn6}	8.4162 A	I_{pk6-}	−12.6376 A
I_{fnd6}	8.5748 A	I_{dc6}	0.0000 A
I_{thd6}	4.752 %	I_{ac6}	8.5860 A
		f_6	59.9978 Hz

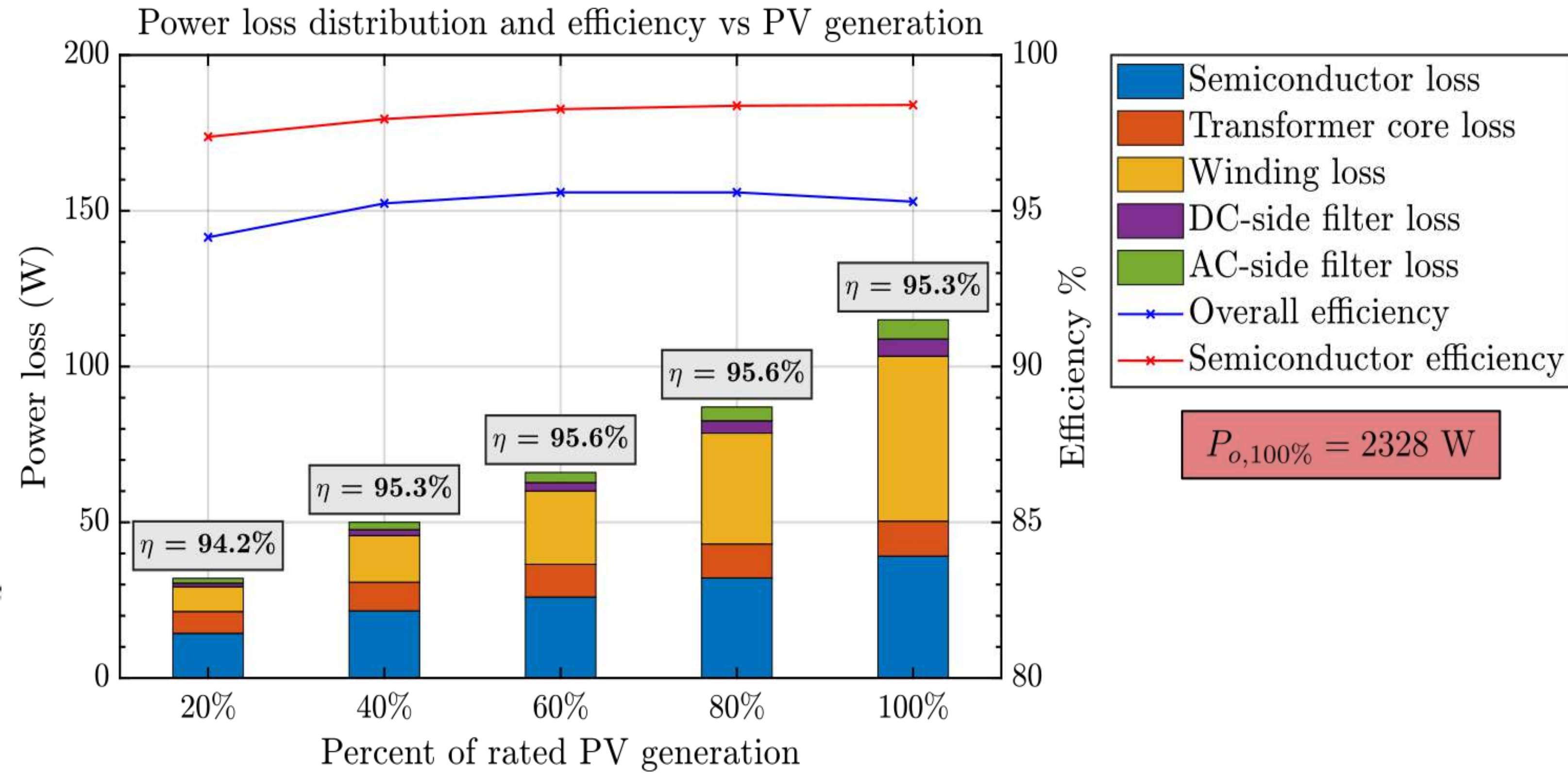
Power factor and current total harmonic distortion at 100% load at 240 V AC voltage.

- Measurement using Hioki Power Analyzer PW6001.
- Current sensors: 50 A, 2 MHz.
- Voltage potentiometers: 1000 V.

2.1 kW, 1-ph grid connected converter prototype enabled by 1200V, 20A SiC BiDFET



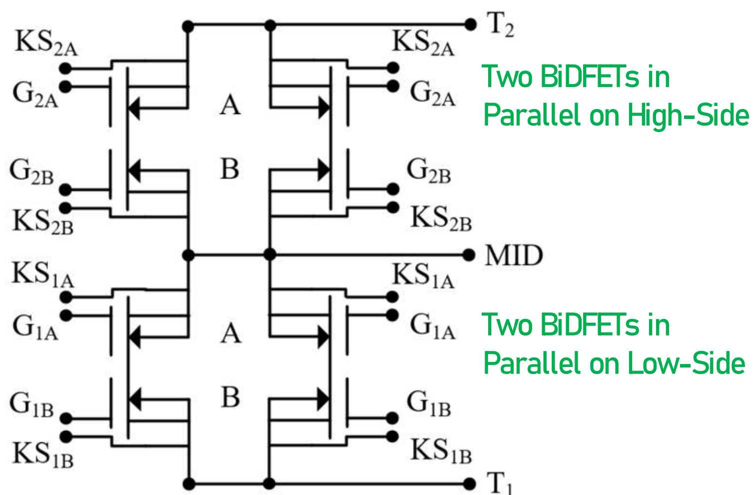
Hardware prototype of the AC/DC DAB converter



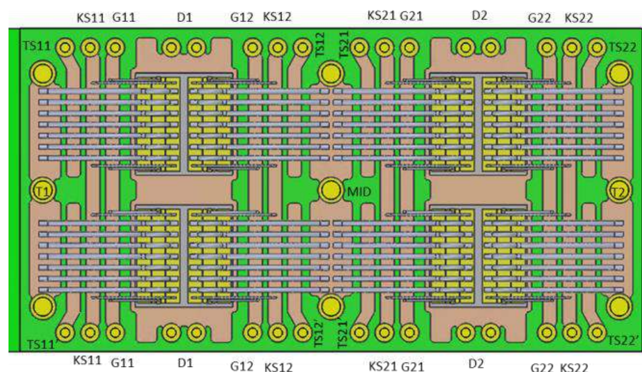
Overall efficiency, semiconductor efficiency and estimated loss distribution at different rates of PV generation.

- Semiconductor efficiency indicates losses in the semiconductors estimated after segregating the transformer, inductor and filter losses.
- Efficiency can be improved by improving transformer design and reducing switching frequency for reduced turn-off losses.

SiC Bi-Directional FET (BiDFET) packaging: 1200V, 50A half-bridge module

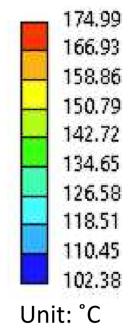


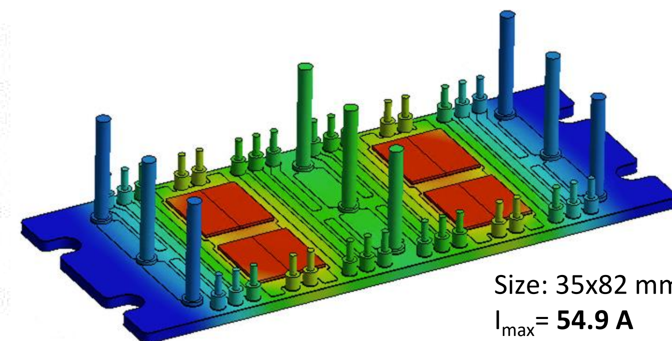
Half-bridge module schematic.



Half-bridge module packaging layout.

Fabricated half-bridge module.

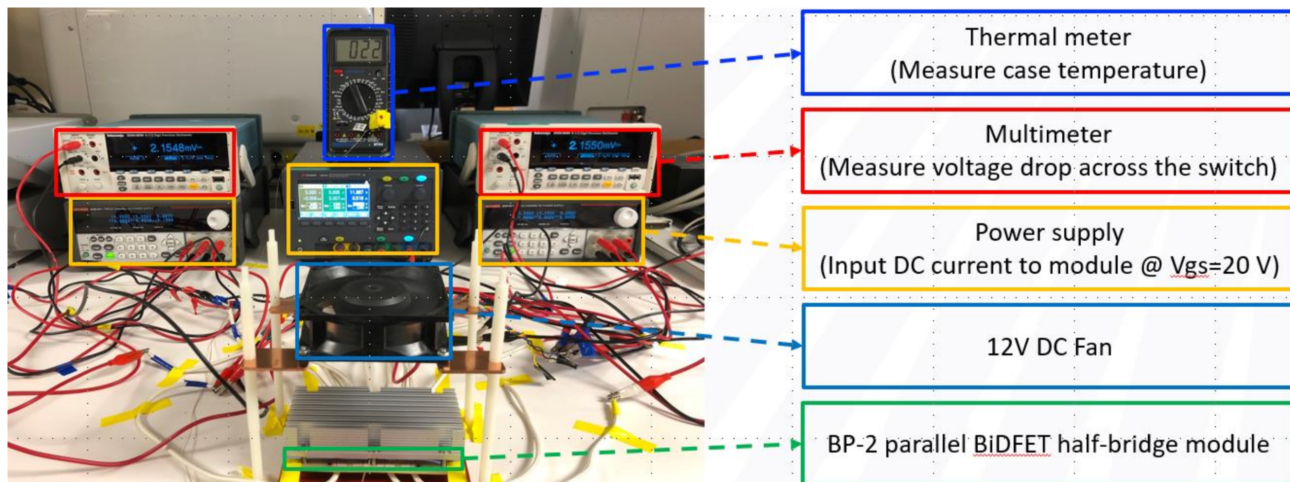




Half-bridge module thermal simulation (h_coeff=750 W/m²K and Ta=25˚C).

- The designed Half-Bridge Module contains two BiDFETs in Parallel per switch to enhance current and power handling capability.
- The package is designed symmetrically to allow for easy installation in the converter.

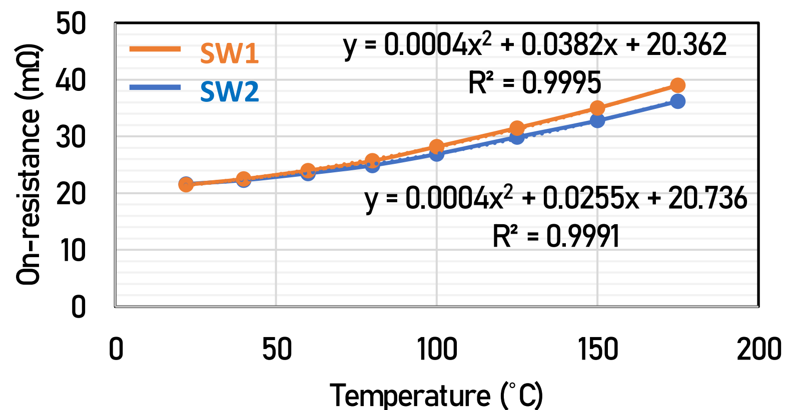
SiC Bi-Directional FET (BiDFET) packaging: 1200V, 50A half-bridge module



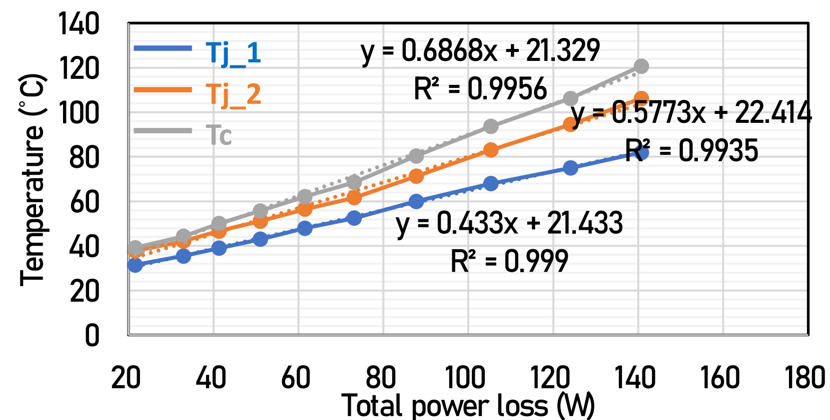
Half-bridge module experimental thermal characterization testbench.

I (A)	V1 (V)	V2 (V)	Ron_1 (mΩ)	Ron_2 (mΩ)	P1 (W)	P2 (W)	P_total (W)	Tc (˚C)	Tj_1 (˚C)	Tj_2 (˚C)
22	0.49	0.49	22.2	22.3	10.8	10.8	21.6	31.5	37.9	39.2
27	0.61	0.61	22.5	22.7	16.4	16.5	32.9	35.5	42.1	44.3
30	0.69	0.69	22.8	23.1	20.6	20.8	41.3	39	46.7	50.0
33	0.77	0.78	23.1	23.5	25.4	25.7	51.1	43	51.1	55.7
36	0.85	0.86	23.5	23.9	30.5	31.0	61.5	48	56.5	62.2
39	0.93	0.95	23.9	24.4	36.2	37.0	73.1	52.5	61.7	68.6
42	1.03	1.06	24.6	25.3	43.2	44.5	87.7	60	71.3	80.4
45	1.15	1.19	25.6	26.4	51.8	53.6	105.3	68	83.0	93.7
48	1.27	1.32	26.5	27.6	60.8	63.2	124.1	75	94.5	106.2
50	1.38	1.45	27.6	29.0	68.6	72.1	140.7	82	106.2	120.7

Experimental thermal characterization testdata.

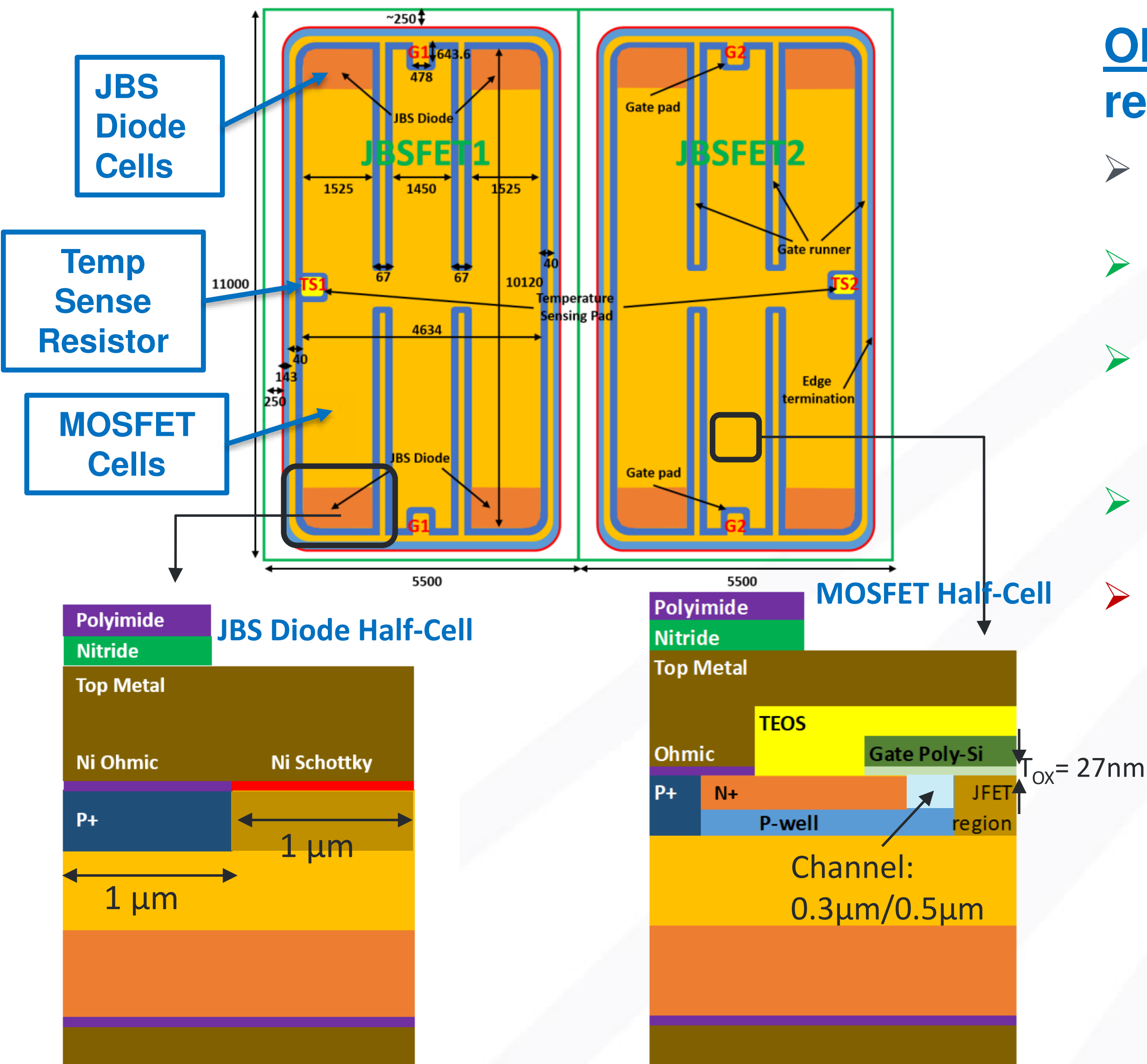


Ron vs temperature



Power loss vs temperature

Gen-2 BiDFET: Chip Design

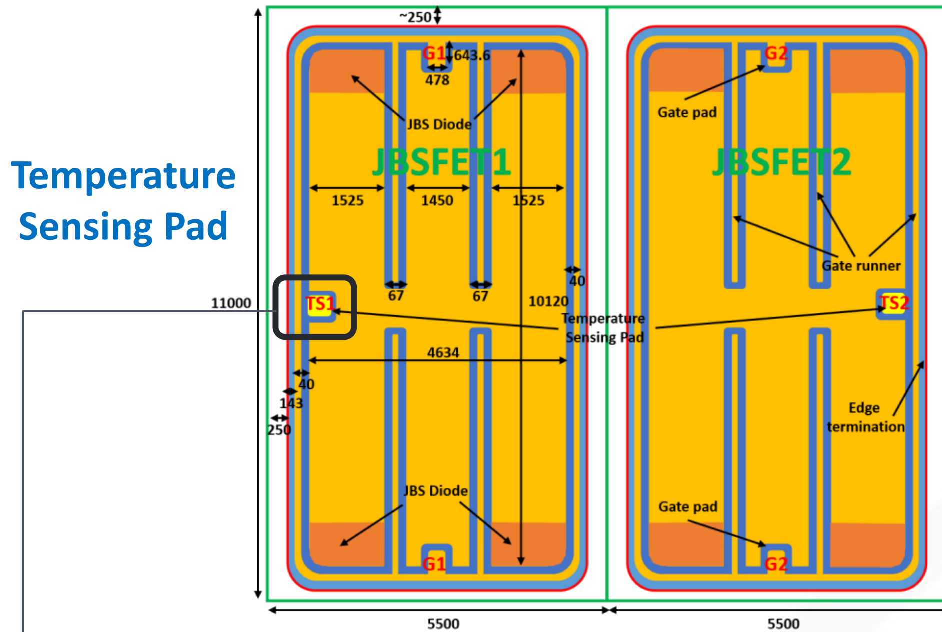


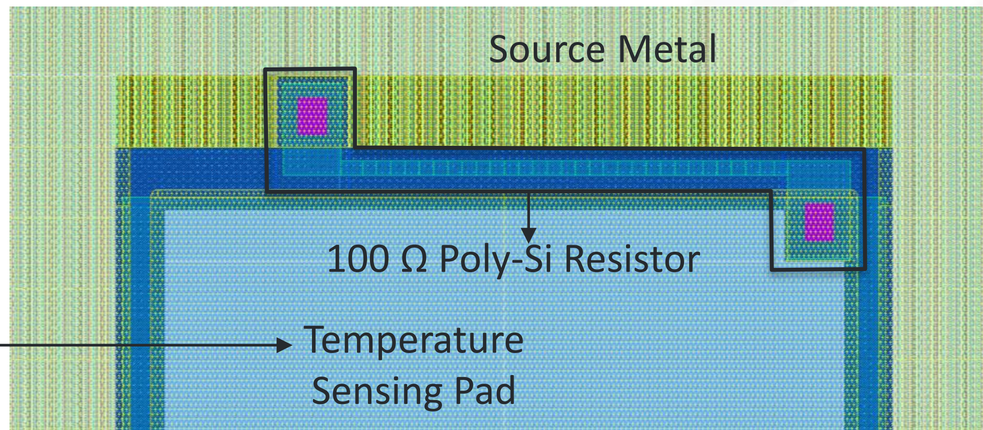
Objective: Improved design with 2x lower specific on-resistance for the same die size.

- Gen-1 BiDFET, with on-resistance of 50 mΩ, has JBS diode integrated within MOSFET cells.
- Gen-2 BiDFET, with on-resistance of 26 mΩ, has JBS diode and MOSFET in separate parts of the JBSFET chip.
- Gen-2 BiDFET On-Resistance further reduction achieved by reducing gate oxide thickness from 55 to 27 nm and reducing channel length from 0.5 µm to 0.3 µm.
- Higher ohmic contact anneal temperature used to further reduce specific on-resistance.
- New BP-2 BiDFET Design has same active area and chip size as the BP-1 BiDFET.
  - JBS Diode Active Area = 0.045 cm^2
  - MOSFET Active Area = 0.405 cm^2
  - MOSFET $R_{on,sp}$ = 5.3 mΩ-cm^2
  - MOSFET R_{on} = 13 mΩ
  - BP-2 BiDFET R_{on} = 26 mΩ
  - BP-2 BiDFET I_{on} = 25 A
  - BP-2 BiDFET V_{on} = 0.65 V @ 25 A

Gen-2 BiDFET: Temperature Sensor

Temperature Sensing Pad





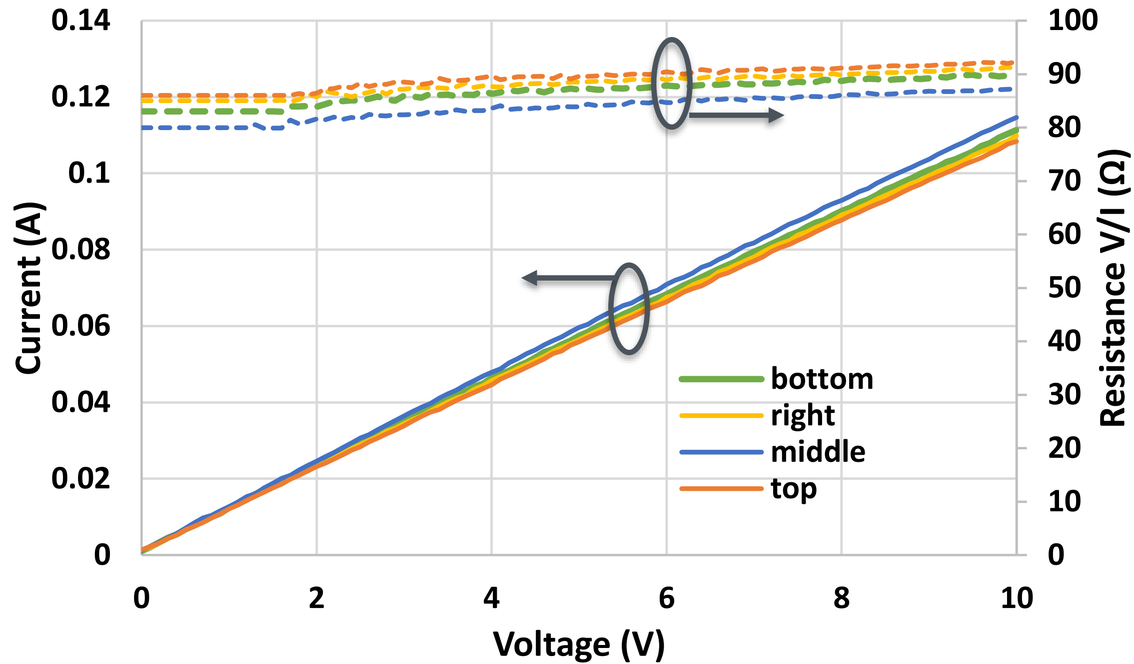
New feature created in Gen-2 BiDFET:
On-Chip Temperature Sensing Capability

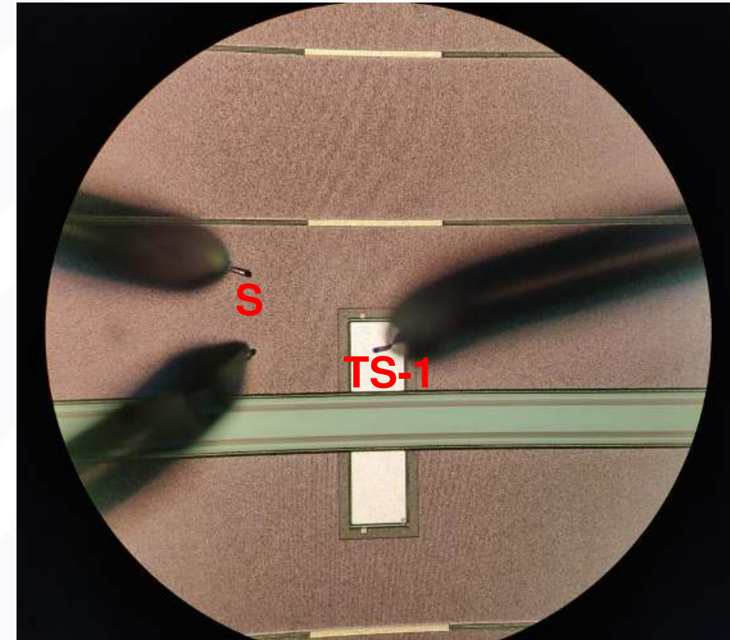
- Makes use of Silicided Polysilicon Gate Electrode Layer
- No additional processing steps required
- Silicided Polysilicon Sheet Resistance: 3 Ω/square

- 100 Ω Poly-Si resistor integrated on-chip to allow BiDFET device temperature monitoring

Temperature Sense Resistor: Uniformity

Sense Resistor Room Temperature Data





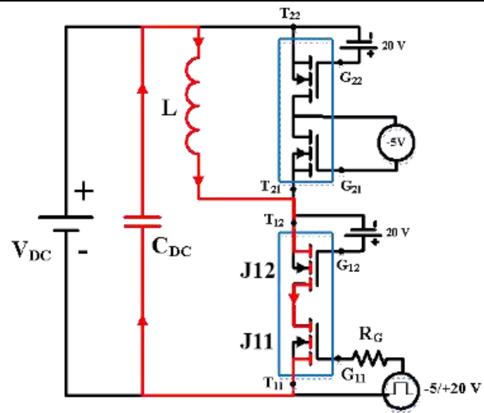
Wafer Position	R
Bottom	90 Ω
Right	91 Ω
Middle	87 Ω
Top	92 Ω

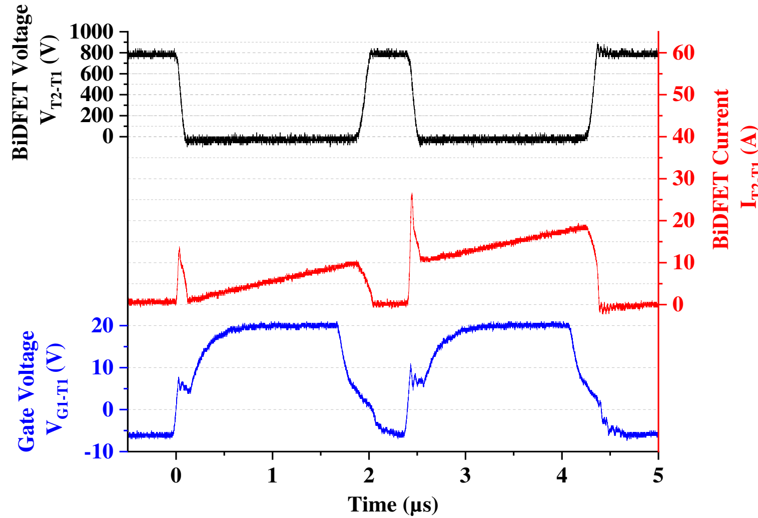
- Measured Temperature Sense Resistance @ RT = 90 Ω
- Matches design value of ~100 Ω
- Achieved project goal

The 1.2 kV BiDFET Switch: Switching Performance

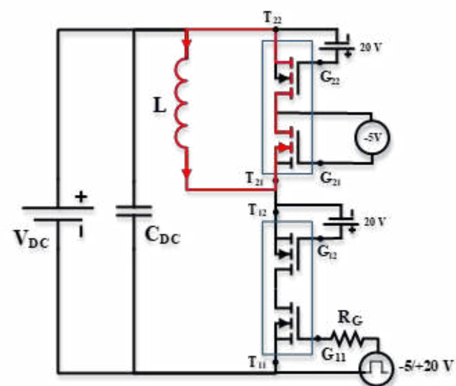
Test Conditions: V_{DC} = 800 V, $I_{T_2T_1}$ = 8-20 A, Case Temperatures: 25 °C, Gate resistances = 10 Ω
LS Switch: 1.2 kV BiDFET ($V_{G_1T_1}$ = -5/20 V, $V_{G_2T_2}$ = 20 V), HS Switch: 1.2 kV BiDFET ($V_{G_1T_1}$ = -5 V, $V_{G_1T_1}$ = 20 V)

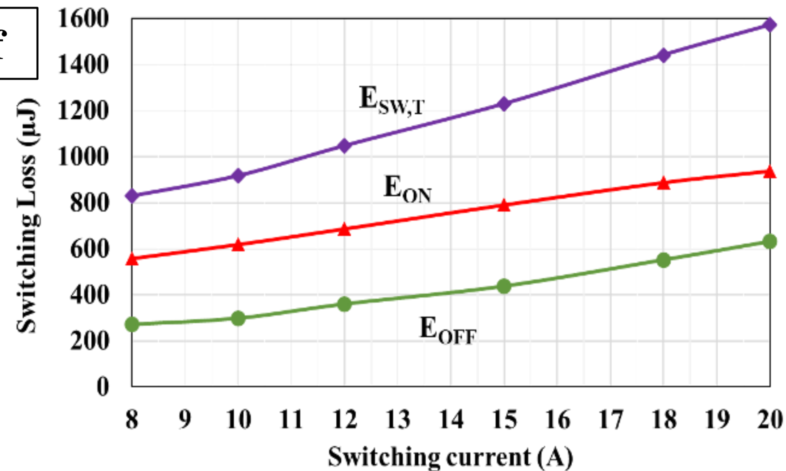
Current Flow Schematics: With Low-side BiDFET G_{11} On





With Low-side BiDFET G_{11} Off





I_{ON} (A)	E_{ON} (µJ)	E_{OFF} (µJ)	$E_{SW,T}$ (µJ)	$E_{SW,T}$ Norm.
8	559	271	**830**	0.9
10	620	298	**918**	1.0
12	688	360	**1048**	1.14
15	792	438	**1230**	1.34
18	889	553	**1442**	1.57
20	939	633	**1572**	1.71

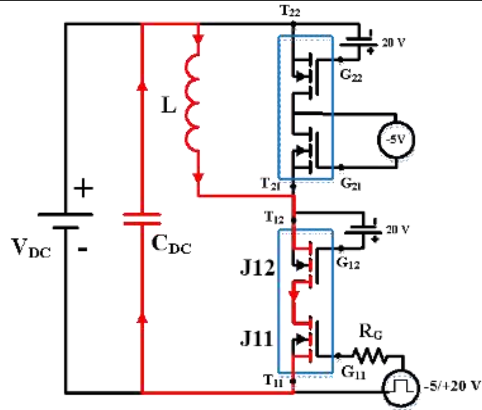
The BiDFET switching losses increase by a factor of 1.71x when I_{ON} rises from 10 to 20 A.

The BiDFET exhibits a current overshoot during turn-on transitions due to output capacitance of HS switch.

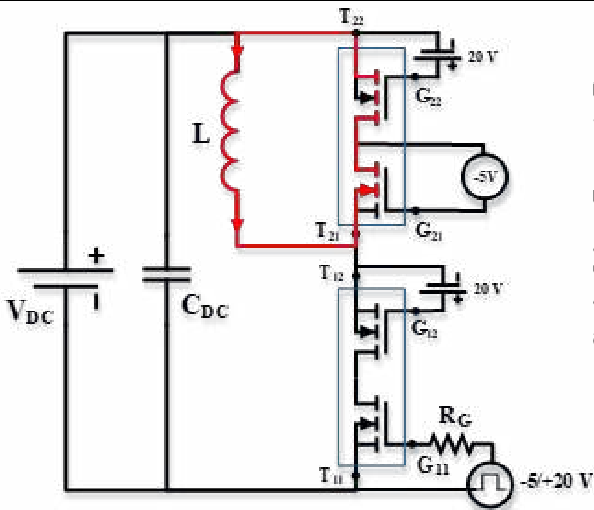
The 1.2 kV BiDFET Switch: Switching Performance

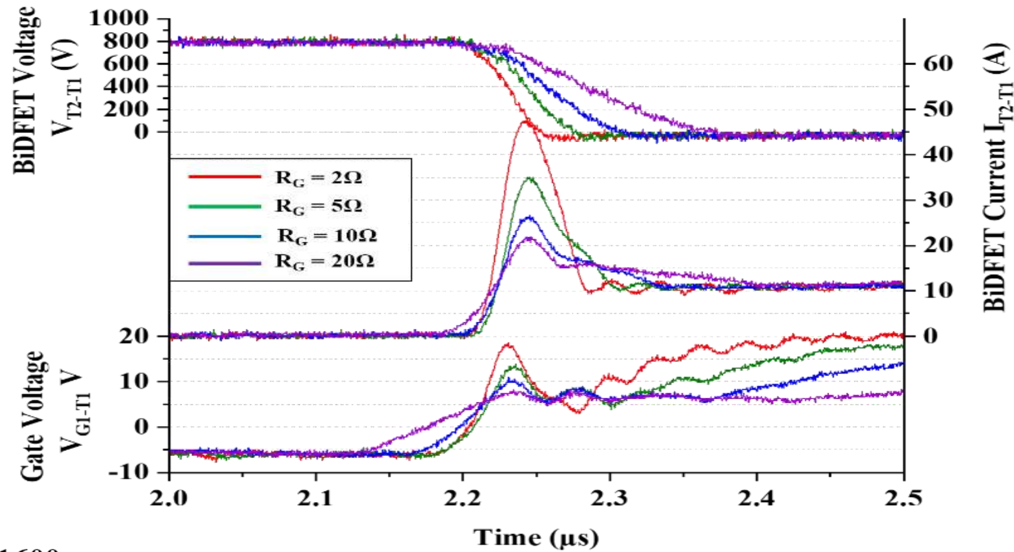
Test Conditions: V_{DC} = 800 V, $I_{T_2T_1}$ = 10 A, Case Temperatures: 25 °C, Gate resistances = 2-20 Ω
LS Switch: 1.2 kV BiDFET ($V_{G_1T_1}$ = -5/20 V, $V_{G_2T_2}$ = 20 V), HS Switch: 1.2 kV BiDFET ($V_{G_1T_1}$ = -5 V, $V_{G_1T_1}$ = 20 V)

Current Flow Schematics: With Low-side BiDFET G_{11} On

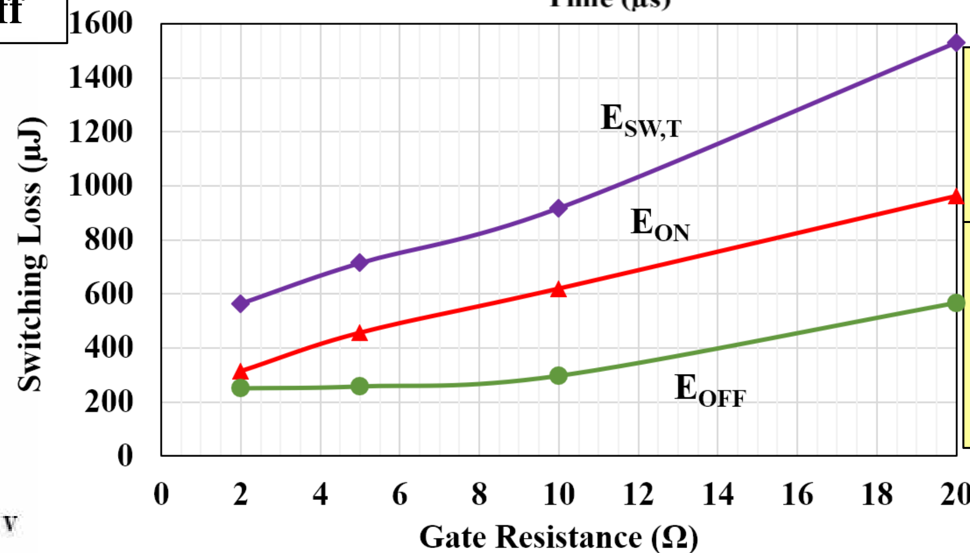


With Low-side BiDFET G_{11} Off





R_G (Ω)	E_{ON} (μJ)	E_{OFF} (μJ)	$E_{SW,T}$ (μJ)	$E_{SW,T}$ Norm.
2	313	252	**565**	**0.62**
5	456	259	**715**	**0.78**
10	620	298	**918**	**1.00**
20	964	566	**1530**	**1.67**



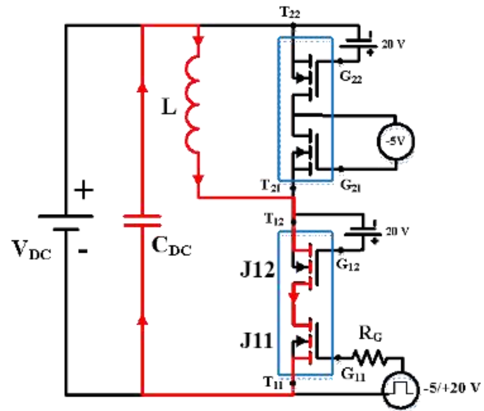
The BiDFET switching losses increase with gate resistance due to increased switching transition time.

Increased gate resistance reduces gate current leading to a slow transient (reduced dV/dt). The slow transients result in a reduced current overshoot at turn-on.

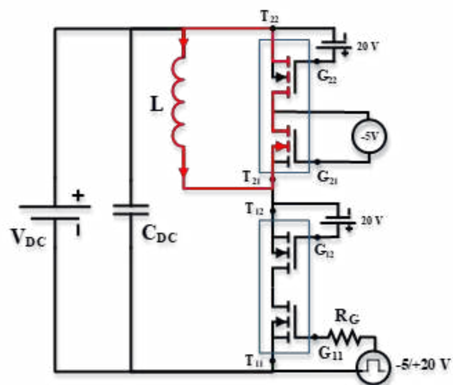
The 1.2 kV BiDFET Switch: Switching Performance – Loss vs Case Temperature

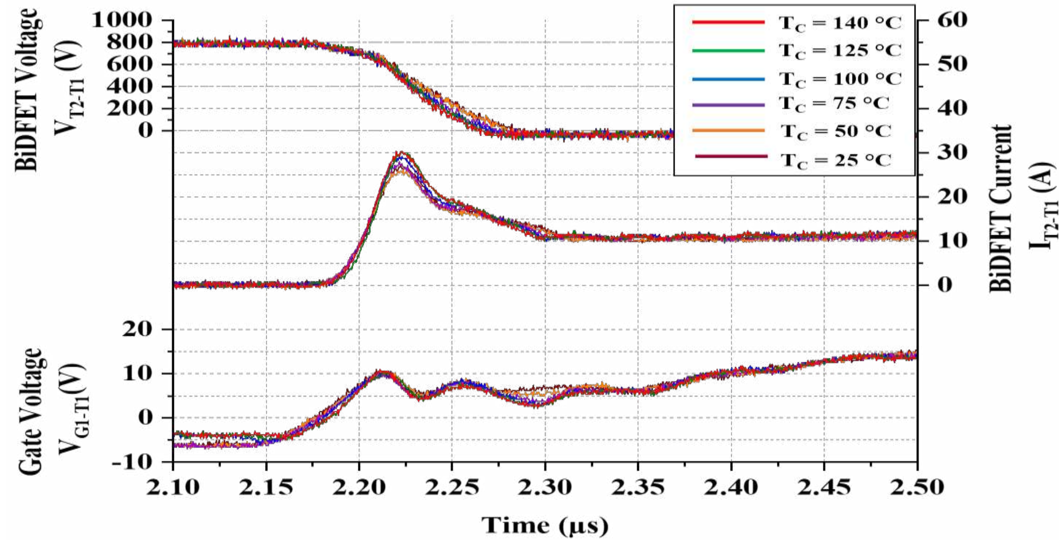
Test Conditions: V_{DC} = 800 V, $I_{T_2T_1}$ = 10 A, Case Temperatures: 25-140 °C, Gate resistances = 10 Ω
LS Switch: 1.2 kV BiDFET ($V_{G_1T_1}$ = -5/20 V, $V_{G_2T_2}$ = 20 V), HS Switch: 1.2 kV BiDFET ($V_{G_1T_1}$ = -5 V, $V_{G_1T_1}$ = 20 V)

Current Flow Schematics: With Low-side BiDFET G_{11} On

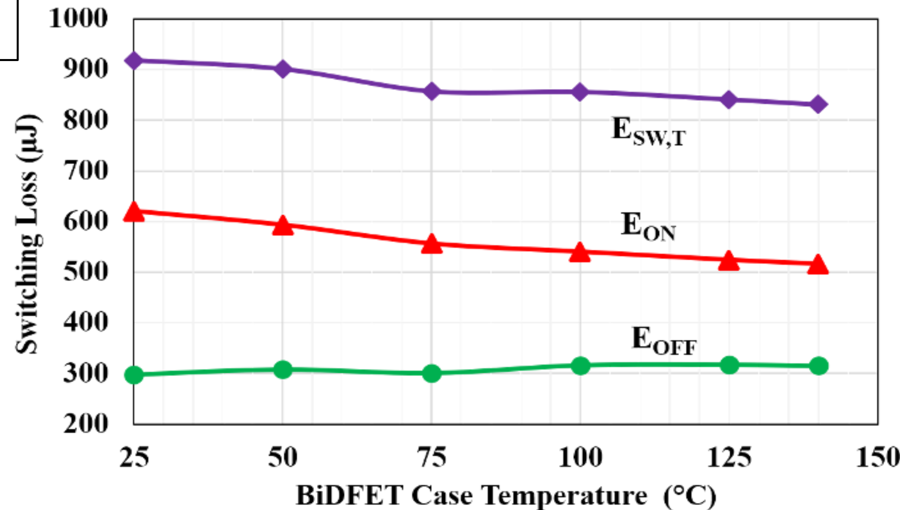


With Low-side BiDFET G_{11} Off





T_C (°C)	E_{ON} (µJ)	E_{OFF} (µJ)	$E_{SW,T}$ (µJ)	$E_{SW,T}$ Norm.
25	620	298	**918**	1
50	593	308	**901**	0.96
75	556	301	**857**	0.9
100	540	316	**856**	0.87
125	524	317	**841**	0.85
140	516	315	**831**	0.83



Reduced output capacitance of the high-side switch results in reduction of switching loss with case temperature.

The BiDFET switching losses decrease by 17% as case temperature increases from 25 °C to 140 °C.

Peak currents at turn-on exhibit small reduction with increasing case temperature.

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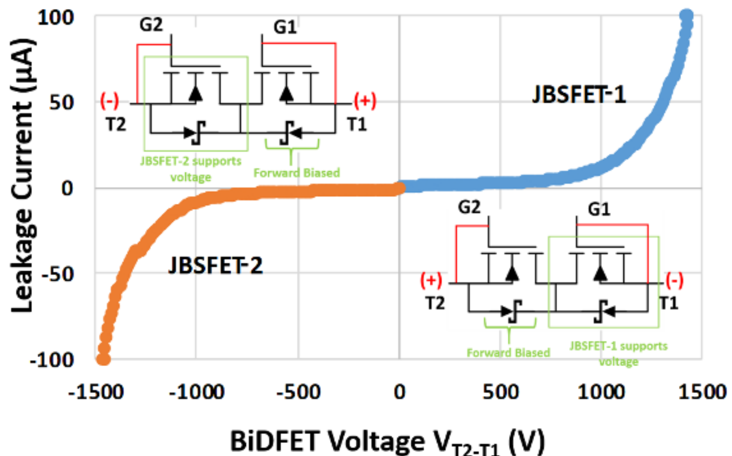
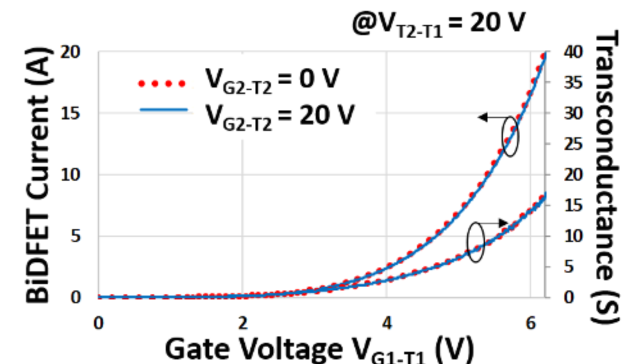
The 1.2 kV BiDFET Switch: Static Characterization

BiDFET blocking characteristics:



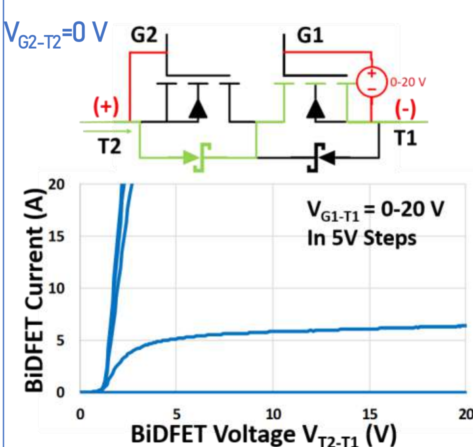
- In 1st quadrant: $V_{G1-T1}=V_{G2-T2}=0$ V, $V_{T2-T1}>0$V, V_{T2-T1} supported by JBSFET-1.
- In 3rd quadrant: $V_{G1-T1}=V_{G2-T2}=0$ V, $V_{T2-T1}<0$V, V_{T2-T1} supported by JBSFET-2.
- BV @ 100 μA > **1400 V** in both 1st and 3rd quadrants.

BiDFET transfer characteristics:

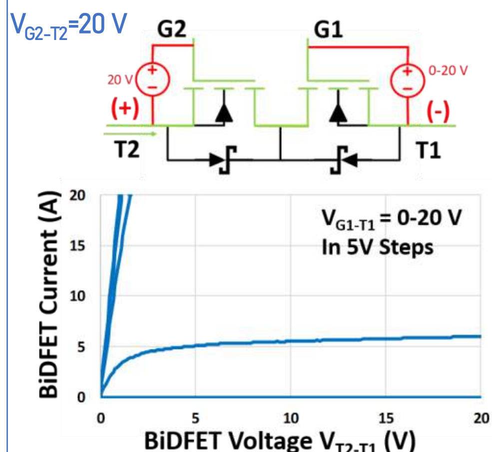


- Conduction through JBSFET-1 channel for both cases.
- V_{th} @ V_{T2-T1}=20 V, I_{T2-T1}=10 mA was **1.35 V**.
- G_m @ V_{T2-T1}=20 V, I_{T2-T1}=20 A was **17 S**.

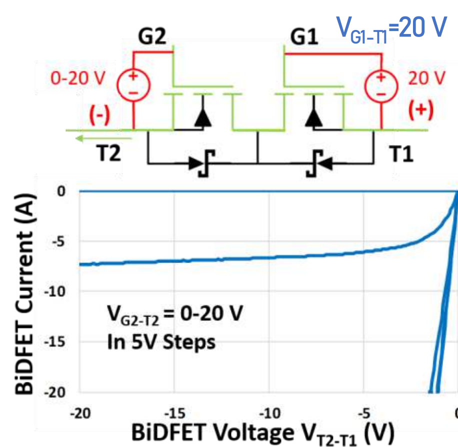
BiDFET output characteristics:



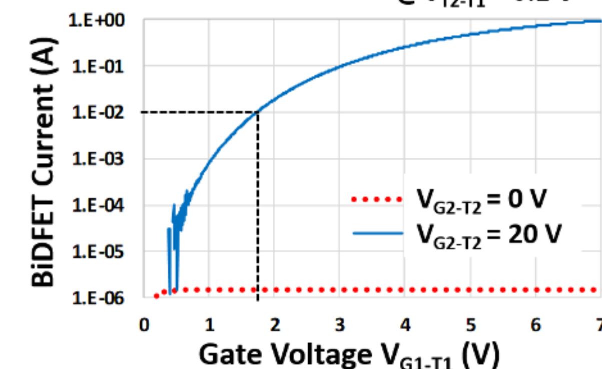
- Conduction through series JBS diode.
- Knee Voltage =**1.2 V**.



- Output characteristics in 1st quadrant for V_{G2-T2}=20V.
- R_{on} @ I_{T2-T1}=10 A and V_{G1-T1}= 20V is **50 mΩ**.



- Output characteristics in 3rd quadrant for V_{G1-T1}=20V.
- R_{on} @ I_{T2-T1}=-10 A and V_{G2-T2}= 20V is **50 mΩ**.



- Conduction through JBSFET-1 & JBSFET-2 channels for V_{G2-T2}=20 V case.
- No conduction for V_{G2-T2}=0 V case, because 0.1 V on T2 is not enough to forward bias internal JBS diode of JBSFET-2.
- V_{th} @ V_{T2-T1}=0.1 V, I_{T2-T1}=10 mA was **1.73 V**.

Acknowlegments:

- Prof. Baliga – SiC BiDFET device
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- Graduate Students:
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- PV converter: Ramandeep Narwal
- Magnetics: Isaac Wong, Sagar Rastogi

- Post-Doc:
- PV Converter Applications: Suyash Shah

- Device Manufacturing:
- X-FAB Foundry: Voshadhi Amarsinghe, John Ransom

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