Progressive Switching of Hybrid DC Circuit Breakers for Faster Fault Isolation

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***Abstract*—Achieving fast and efficient circuit protection is critical to direct current (DC) system safety with many scholars focusing on hybrid direct current circuit breakers (DCCBs) to achieve this goal. However, fault isolation speed is limited by the time required for the mechanical switch to achieve sufficient dielectric strength across the contacts. In this paper, we propose a progressive solid-state switching method for hybrid DCCBs to dynamically control the voltage potential across the mechanical switch. The proposed switching method reduces fault isolation time and limits the peak fault current during breaker operation. DC system dynamics are explored and the voltage withstand capability of a new Ultrafast Mechanical Switch is analyzed. The discovered characteristics are used to design a progressive switching method in computer simulation and it is validated experimentally with a test prototype. In the proposed design fault current is curtailed during the mechanical switch opening sequence rather than waiting until it is fully open, improving system stability.**

***Index Terms*—Circuit breakers, microgrids, power system protection, direct current, dc distribution, fault isolation, current limiting, mechanical switch, hybrid dccb**

NOMENCLATURE

CS	Commutating switch
DCCB	Direct current circuit breaker
DSP	Digital signal processor
LVDC	Low voltage direct current
MB	Main breaker
MMF	Magnetomotive force
MOSFET	Metal oxide field effect transistor
MOV	Metal oxide varistor
MVDC	Medium voltage direct current
TCA	Thomson coil actuation
TIV	Transient interruption voltage
UFMS	Ultrafast mechanical switch
VSC	Voltage source converter

I. INTRODUCTION

Increasing interest in distributed renewable energy resources has led to direct current (DC) circuit protection research becoming increasingly prevalent [1]–[4]. The lack of natural current zero crossing in DC and other variable current applications prevents natural arc extinction during mechanical contact separation [2]. This sustained arcing is addressed using large, expensive electromechanical switchgear, or smaller and faster solid-state switches which consume real power [4], [5]. A combination of these two topologies is known as a hybrid direct current circuit breaker (DCCB). This design exploits the benefits of each by providing a low resistance mechanical contact coupled with high-speed semiconductor switches [6], [7]. Together, these topologies seek to achieve high speed and high-efficiency DCCBs [8], [9].

Hybrid DCCBs, illustrated in Fig. 2, provides a low resistance current path through the ultrafast mechanical switch (UFMS) and commutating switch (CS) during normal operation. To isolate a fault, the CS directs current flow to the parallel solid-state branch known as the main breaker (MB), allowing the UFMS to open under a zero-current condition which prevents arcing. Once adequate dielectric strength is established across the contacts of the UFMS current flow is interrupted by the MB. The solid-state branch is made of high voltage power semiconductor devices which can isolate current flow in several microseconds (μsec). However, the speed of semiconductor switches sacrifices efficiency due to high conduction losses [10], [11]. New press-pack devices such as the insulated gate bipolar transistor (IGBT), injection-enhanced gate transistor (IEGT) and integrated gate commutated thyristor (IGCT) can interrupt tens of kiloamps, expanding MB capabilities [12]. Because the overall operation time of a hybrid DCCB is dependent upon the mechanical switch speed, fault current continues to rise throughout the entire opening sequence.

For the rest of this paper, in Section II the fault characteristics of DC distribution are assessed and the unique protection requirements analyzed. This section then reviews the challenge of the hybrid DCCB and describes the operation of the circuit breaker, illustrating the need for innovation. The proposed progressive switching of hybrid DCCBs is then presented in Section III in analytical form, and the concept is tested in computer simulation. In Section IV, the design process of each hybrid DCCB subsystem and the coordination of the subsystems is assessed. The experimental results of the test prototype are presented in Section V to validate the analytical and simulation models. Finally, Section VI discusses the significant findings of the progressive switching method, and summarizes the key contributions made by the progressive switching of the hybrid DCCB.

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II. DC Protection

To address the challenges of DC distribution system protection, in this section, DC fault characteristics are analyzed and the hybrid DCCB topology is reviewed.

A. DC Distribution Fault Characterization

While UFMS actuation has become very fast, the operation time of the switch and dissipation of the voltage surge felt across the DCCB limits the isolation time [13], [14]. This voltage surge, due to stored system energy, exceeds the nominal voltage rating during fault isolation [3]. DC systems have lower inductance than alternating current (AC) systems due to inverter decoupling of motor windings, replacement of the power transformer with power electronics, and smaller transmission distances [3]. Therefore, DC fault current rises faster than in AC systems, requiring faster protection. Current-limited voltage source converters (VSCs) most commonly supply DC distribution systems. Voltage collapse occurs quickly in these systems because converters are unable to supply fault current the way conventional rotational generation can [15]. Therefore, DC distribution systems require high-speed fault current isolation and localized fault current limiting [9].

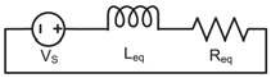

Fig. 1. Simplified analytical model of a hybrid DCCB

The simplified equivalent circuit of a hybrid DCCB is shown in Fig. 1. This model includes the voltage source V_s, equivalent line inductance L_{eq}, and equivalent resistance of the on-state losses and contact resistance, R_{eq}. Solving for voltage, this gives $V_s = L_{eq}\frac{di(t)}{dt} + R_{eq}i(t)$. If a pre-fault current I_0 is assumed with some value between $+I_{max}$ and $-I_{max}$, the value of fault current and fault current derivative are given by

$$i(t) = \frac{V_s}{R_{eq}} + \left(I_0 - \frac{V_s}{R_{eq}}\right) e^{-\left(\frac{R_{eq}}{L_{eq}}\right)t}, \tag{1}$$

$$i'(t) = \left(-\frac{R_{eq}}{L_{eq}} I_0 + \frac{V_s}{L_{eq}}\right) e^{-\left(\frac{R_{eq}}{L_{eq}}\right)t}. \tag{2}$$

Proper component selection and system design results in a very low value of R_{eq}. For $R_{eq} \approx 0$, the current derivative is given by $\frac{V_s}{L_{eq}}$, resulting in a linear fault current rise. This high $\frac{di}{dt}$ fault current rise will quickly exceed the current limitations of the connected VSCs. To protect themselves, the VSCs then enter constant current mode, also known as current limiting. This transition can cause a rapid and cascading voltage collapse of the connected system if the short circuit fault persists [16].

B. Isolation Speed Challenge with Hybrid DCCBs

A hybrid DCCB consists of two parallel branches. One consists of semiconductor switches only, known as the MB. The parallel conduction path consists of the CS and UFMS, the two being connected in series. The later branch functions as the load current conduction path during normal operation. The fault isolation procedure, while variable by design, consists of the following steps illustrated in Fig. 2:

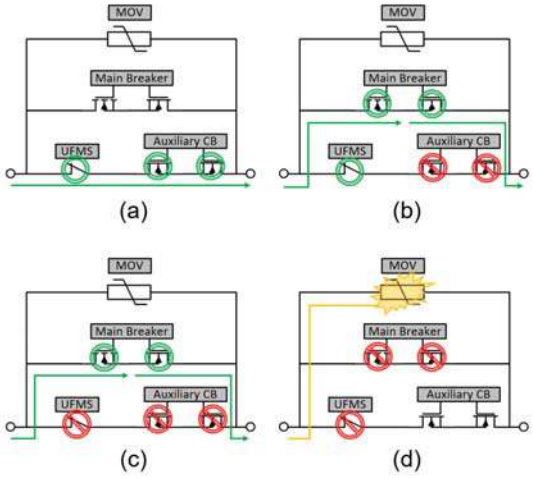

Fig. 2. Opening sequence of a hybrid DCCB

(a) During normal operating condition, current passes through the UFMS and CS.
(b) Once a fault is detected, the MB turns on and the CS turns off, commutating load current to the MB within several μsec.
(c) While load and fault current are flowing through the MB, the UFMS opens with zero current flow, preventing arcing.
(d) When the dielectric strength of the vacuum gap in the UFMS can withstand the transient interruption voltage (TIV) the MB turns off, stopping current flow and isolating the fault. The voltage surge due to system inductance is clamped and excess energy is absorbed by the surge arrestor which most commonly is a Metal Oxide Varistor (MOV).

This operation sequence provides minimal on-state power consumption during normal operation in (a) coupled with fast, arc-free current isolation with the MB in (d). Idealized current and voltage waveforms, and the dielectric strength of a UFMS across a typical hybrid DCCB are shown in Fig. 3. These waveforms correspond to the steps explained in Fig. 2, with significant events occurring at times t_0 through t_5.

$t0$ A downstream overcurrent fault initiates from normal operating condition prior to $t0$.
$t1$ Fault current reaches the trip setpoint, beginning the protective action sequence.
$t2$ The CS turns off which commutates the fault current to the MB and the UFMS begins opening and increasing the vacuum gap dielectric strength.
$t3$ The UFMS contacts gain sufficient separation and the MB turns off.
$t4$ Voltage across the DCCB quickly rises until it is

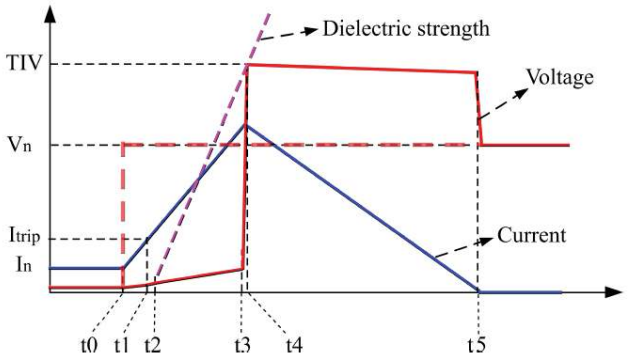

Fig. 3. Operation of a hybrid DCCB

clamped by the MOV and the excess system energy is absorbed by the MOV.

$t5$ Excess energy has been absorbed, fault current dissipated to zero, and the system is fully isolated.

Analysis of Fig. 3 and the current calculations given by (1) and (2) illustrate that the isolation time of a hybrid DCCB is restricted by the millisecond ($msec$) operation time of the UFMS. Fault current continues to rise in the system until adequate dielectric strength is achieved to withstand both nominal system voltage and the TIV across the DCCB due to system inductance and stored capacitance being dissipated.

III. Proposed Progressive Switching of Hybrid DCCBs

In this paper, we present a new solid-state branch design and progressive switching method which curtails fault current in the MB while the UFMS opening sequence occurs. Curtailing fault current reduces the fault isolation time of hybrid DCCBs by limiting the peak fault current I_{peak}, which subsequently requires less energy absorption by the clamping action of the MOVs. Progressive switching of the MB provides several key features to enhance DC distribution system protection:

- Protects connected electronics by limiting the current peak observed by the system.
- Reduces fault isolation time by quenching the energy surge faster.
- Minimizes the energy absorption requirements of the connected MOV surge arrestors, prolonging their lifespan.
- Naturally balances the energy of series-connected power semiconductor devices by separating them into stages.
- Prevents voltage collapse of the entire distribution system by providing localized current limiting.
- Enables tertiary features such as soft-start of downstream equipment.

The progressively switched hybrid DCCB functional block diagram is shown in Fig. 4, and the simplified schematic is shown in Fig. 5. This new approach at hybrid DCCBs sequentially turns off the 1^{st}, 2^{nd}, 3^{rd}, and so on up to the n^{th} stage of series-connected semiconductor switches in the

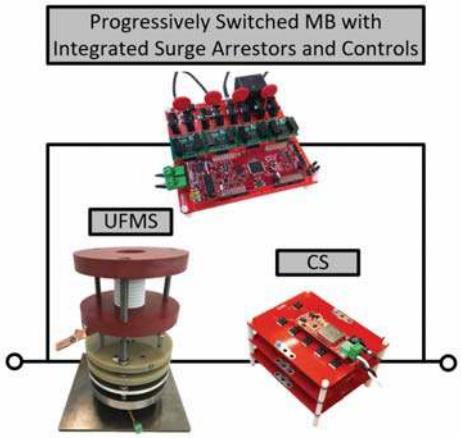

Fig. 4. Progressively switched, actively damped UFMS hybrid DCCB functional diagram

MB. This process incrementally steps up the voltage across the circuit breaker to match the UFMS dielectric strength and limit fault current.

The incremental voltage steps, that are shown in Fig. 6, correspond with the UFMS displacement during the opening sequence, and therefore, align with the combined dielectric strength of the UFMS vacuum chamber V_{ds}, and the blocking voltage of the CS V_{cs}, balancing the two branches of the hybrid DCCB to minimize the I_{Peak} observed during fault isolation.

Compared to the fault isolation stages of the hybrid DCCB discussed in Section II-B, progressive switching of the MB has several extra control steps. Initially, the sequence starts the same from $t0$ through $t2$. However, after the breaker controller sends the gate signal to open the UFMS with active damping, it does not wait for the switch to fully open prior to turning off the MB. Depending on the dielectric medium, the UFMS gains a specific voltage withstand capability proportional to contact displacement. Once this matches the blocking voltage rating of the first stage MOV, the controller turns off the corresponding switch. The fault current now flows through the first stage MOV and rest of the on switches. As the UFMS contact displacement grows, the controller turns off each

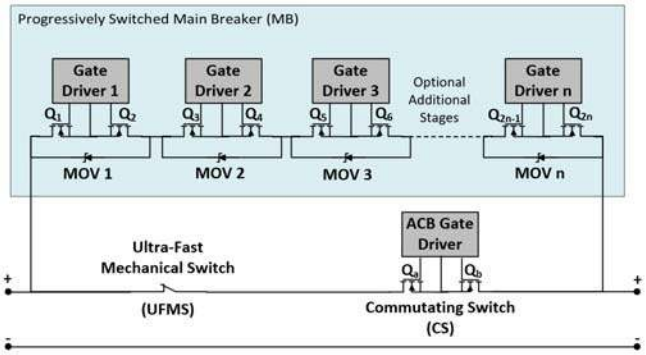

Fig. 5. Progressively switched hybrid DCCB schematic

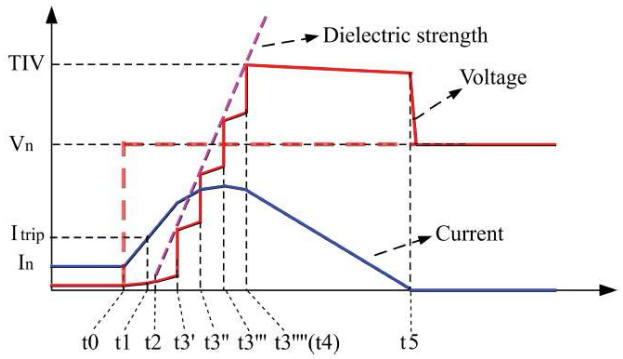

Fig. 6. Operation of proposed progressive hybrid DCCB

semiconductor switch stage matching the dielectric strength of the UFMS and the MOVs placed across the MB. This is illustrated in Fig. 6.

- $t0$ - $t2$ Same Operation as in the single-stage hybrid. Normal operation before $t0$ where the fault occurs, the trip setpoint is reached at $t1$ and the CS turns off and UFMS starts opening at $t2$.
- $t3'$ The controller determines the UFMS dielectric strength is capable of withstanding V_{stage1} and turns off the stage 1 solid-state switch. This begins to curtail fault current and absorb energy in MOV 1.
- $t3''$ - $t3^n$ As the dielectric strength of the UFMS continues to rise, each subsequent solid-state switch stage in the MB is turned off to correspond with the $V_{stage(n)}$ for that stage.
- $t4$ Once all n stages have been switched off, the remaining energy due to system inductance is dissipated by the MOVs in each stage, now all connected in series.
- $t5$ Same Operation as in the single-stage hybrid. Excess energy has been absorbed, fault current dissipated to zero, and the system is fully isolated.

Coordinating progressive switching of the MB with the dielectric strength in the UFMS allows the current isolation process to begin as soon as sufficient vacuum gap exists. This principle is illustrated in a hybrid DCCB simulation with a 2 ms UFMS in Fig. 7. The green trace shows a 400% nominal I_{peak} is sustained by the simulated single-stage hybrid DCCB. In a single-stage hybrid DCCB, the UFMS must fully open prior to isolation of fault current. However, a four-stage progressively switched MB under the same test conditions only observes a 225% current spike and isolates fault current 28% faster than a single-stage operation as observed with the yellow current trace. Furthermore, an eight-stage progressively switched MB isolates 45% faster and I_{Peak} is reduced to 180% nominal current flow. While a higher number of stages isolate fault current faster and minimize energy absorption required, additional cost and DCCB complexity are considered when selecting the number of progressively switched stages.

The transient current observed in Fig. 7 is described in (3) during progressive shutdown. V_s represents the source voltage

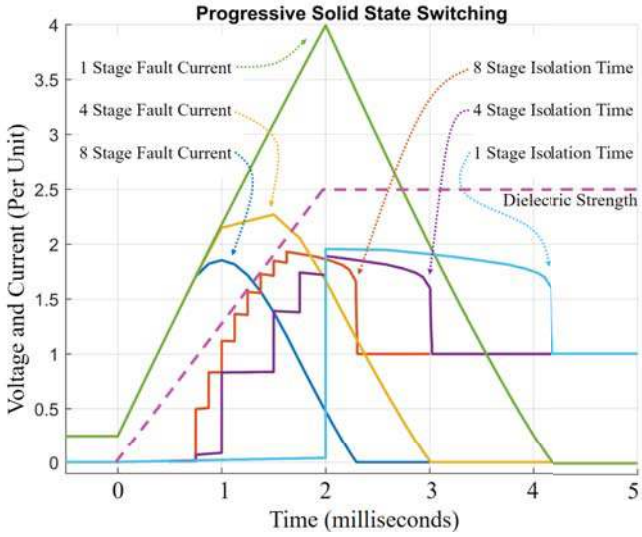

Fig. 7. Simulation of 2ms UFMS operating in a 1 stage hybrid DCCB, and 4 stage and 8 stage progressively switched hybrid DCCBs

where the voltage across each stage is $\Delta V_s = V_s - \sum_{k=1}^{n} V_k$, where V_k and R_k model the MOV voltage drop and leakage current resistance, respectively. $R_n = R_{Load}||R_{Fault} + \sum_{k=1}^{n} R_k$, and finally, t_n is the time when the n^{th} switch turns off.

$$i(t) = \left(i(t_n) - \frac{\Delta V_s}{R_n}\right) e^{-\frac{R_n}{L_{eq}}(t-t_n)} + \frac{\Delta V_s}{R_n} \tag{3}$$

Using the progressive switching method, the voltage differential is coordinated between the solid-state and mechanical switches. Using (3) the number and voltage level of stages is optimized to match the UFMS dielectric strength. The semiconductor switches start limiting fault current up to 1.3 ms earlier than a single-stage hybrid DCCB. As a result, they completely isolate the fault 1.3 ms and 1.9 ms faster with four- and eight-stages, respectively. Therefore, the fault current is curtailed while the UFMS opens, protecting connected converters, and increasing system stability. The DCCB was simulated in PSCAD, as shown in Fig. 8, and the control was

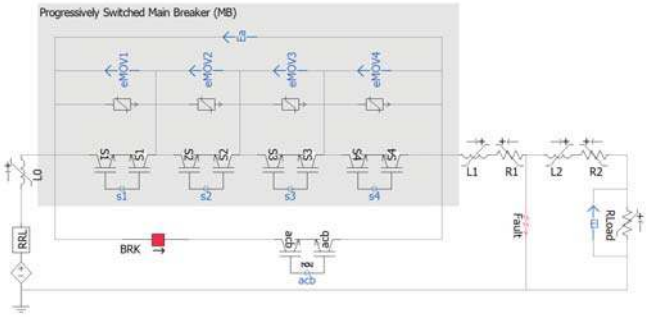

Fig. 8. Simulation of progressively switched DCCB

integrated and tested in PLECS Processor-in-the-Loop (PIL), to test fault detection and control algorithms in real-time.

As the semiconductor switches progressively turn off, the MOVs appear in the main current conducting path. This creates a piecewise linear function. The MOVs are modeled as an ideal diode, a blocking voltage, V_k, and leakage current resistance, R_k. Each additional MOV reduces the slope of fault current rise as the semiconductor stages turn off which reduces the fault current peak. The peak current is given by $\frac{V_s - \sum_{k=1}^{n} V_k}{L_{eq}}$, where n is the switch number and can be observed in Fig. 6 and Fig. 7. This reduces the fault current peak. When the last stage turns off and all transient energy has been absorbed, the current falls to zero.

IV. Prototype Design

To validate the analytical and simulation work completed in Section III, a test prototype was developed and tested in the laboratory. Subsections IV-A, IV-B, and IV-C describe the prototype design and construction for the MB, UFMS, and CS. Finally, the controls, communication, and onboard sensing are presented in Subsection IV-D.

A. Progressively Switched Main Breaker

An onboard digital signal processor (DSP) operates four individual gate driver circuits where each gate driver operates a pair of common-source connected Metal Oxide Field Effect Transistors (MOSFETs) to provide fast switching and simplicity in bidirectional power flow [17]. Unipolar devices, such as MOSFETs, provide fast switching time and low on-state resistance ($R_{ds,on}$). To achieve isolation well into the medium voltage (MVDC) range of 3.2 kV - 69 kV, bipolar devices, such as IGBTs, IEGTs, and IGCTs with a constant voltage drop per module are required. Progressive switching of the MB naturally balances the voltage across devices in series to achieve higher blocking voltage while maintaining protection of each device [18].

The MOV varistor voltage curve dictates the magnitude of each sequenced voltage step. These curves are non-linear and, therefore, each voltage step is a range of isolation, rather than an exact level. MOVs are subject to degradation over time and cycling [19]. Progressive switching reduces the amount of energy that must be absorbed by the overall MOV network during isolation by minimizing the overshoot of fault current. The MOVs used in the prototype are rated to withstand 20 times more energy per cycle than the worst case isolation scenario of the conditions listed in Table II. MOVs can be connected in parallel for additional energy absorption capacity at an incremental cost. Finally, the shutdown sequence of the stages is rotated each operation through the control to ensure equal stress and wear on the four stages of the DCCB.

Fig. 9. Four-stage progressively switched MB

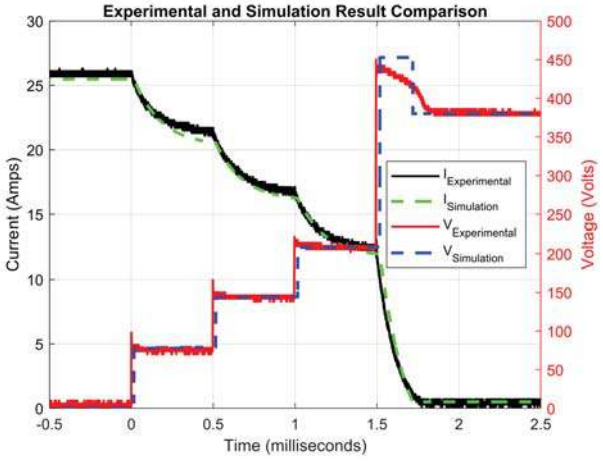

Fig. 10. Four-stage progressively switched MB experimental test waveforms

Standalone solid-state testing results of the progressively switched MB and comparison to simulation are shown in Fig. 10. The MB was tested in a 380 volt, 25 amp, 1.5 ms isolation sequence, experimentally validating the simulation and analytical analysis [18]. The progressive switching method holds true and can be extended to the MVDC voltage level. Commercially available power semiconductor devices like IGBT modules are available with voltage and current ratings in excess of 6.5 kV and 3.6 kA, respectively. The advantages of progressive switching are more significant at these voltage and current levels as the mechanical operation time of UFMS devices for MVDC is longer than for LVDC.

B. Actively Damped Ultrafast Mechanical Switch

The UFMS analyzed utilizes an innovative actively damped Thomson Coil Actuator (TCA) to open a vacuum interrupter and provide adequate dielectric strength for medium voltage applications within 1-3 ms [20]. The rated vacuum of commercial vacuum interrupters is 10^{-5} Pascals (Pa) or 10^{-7} Torr corresponding to a dielectric strength of 20-40 $\frac{kV}{mm}$. Table I illustrates key isolation points in the UFMS as shown in Fig. 11.

Actively damped Thomson Coil actuation is achieved through discharging the energy of a capacitor bank through a small number of turns in the opening coil of the actuator. This

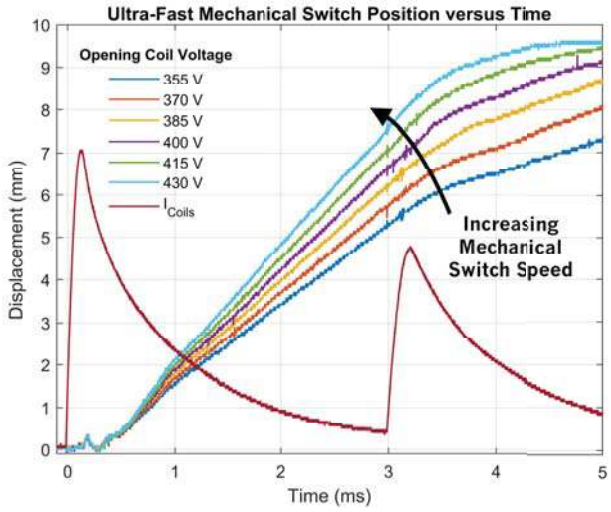

Fig. 11. UFMS vacuum gap vs. time

TABLE. I. Dielectric Strength of UFMS

Time	Displacement	Dielectric Strength
1.0 ms	2.0 mm	40 kV
2.0 ms	5.0 mm	100 kV
3.1 ms	8.0 mm	160 kV

action generates a strong magnetomotive force (MMF) where $MMF = NI$ and I is several kiloamps. The generated field cuts through a conductive copper disk connected to the vacuum interrupter movable contact. The copper disk generates eddy currents creating an MMF in the opposite direction of the coil and a strong repulsive force. This action accelerates the movable mass in the open direction. As the contacts approach fully open, a second capacitor bank discharges through the closing coil. This absorbs the majority of the kinetic energy and helps bring the movable mass to a resting position with its mechanical spring [20].

C. Modular Commutating Switch

The CS, also known as an auxiliary circuit breaker (ACB) or Load Commutating switch (LCS), is located in series with the UFMS to commutate load or fault current to the MB during isolation. The CS must have a low on-state resistance or voltage drop to minimize power consumption, but be capable of commutating current to the MB during any fault condition.

The modular CS designed for the progressively switched hybrid DCCB can be expanded incrementally to meet the nominal current and power consumption requirements for a given application. The CS utilizes parallel MOSFETs connected in a common-source configuration for high efficiency and bidirectional power flow. The on-state power consumption of the CS is a function of the on-state resistance of the MOSFET array with n_{ser} MOSFETs in series and n_{par} MOSFETs in parallel and current, I. Therefore, the total hybrid DCCB efficiency including the UFMS contact resistance is given in (4) where the instantaneous power level of the DCCB is $P_{dccb} = V_s I^2$.

$$\eta = 1 - \left(\frac{I^2 \left(\frac{R_{ds,on} n_{ser}}{n_{par}} + R_{ufms} \right)}{P_{dccb}} \right) \tag{4}$$

The rated blocking voltage of the CS is designed to ensure full commutation of fault current to the MB under all conditions. For MOSFET unipolar devices, $R_{ds,on}$ causes the voltage drop across the MB to rise linearly in proportion to the fault current, and therefore, the CS must be able to block a voltage high enough to overcome $I_{peak} R_{eq}$ of all stages in series. For IGBT bipolar devices with forward voltage drop, V_f, and body diode forward voltage, V_{bd}, the CS must overcome $\sum V_f + V_{bd}$.

D. Integrated Sensing, Communication, and Breaker Controls

The control for progressive switching of a hybrid DCCB is executed via the logic flow-chart shown in Fig. 12. Here, I_{Thresh} depicts the overcurrent threshold, I_{trip} or $\frac{di}{dt}$ rate that will initiate the fault isolation process. $V_{withstand}$ is the dielectric strength of the UFMS as its contacts open. The stage index, n, and the total number of stages, n_{max}, control which stage is under operation. With integrated voltage and current sensors, the onboard controls can be programmed to provide a wide array of protective functions including:

- Manual Open and Manual Close
- Overcurrent
- Rate of current rise $\left(\frac{di}{dt}\right)$
- Undervoltage
- Ground fault current interruption (GFCI)
- Over or under power (kW) trip

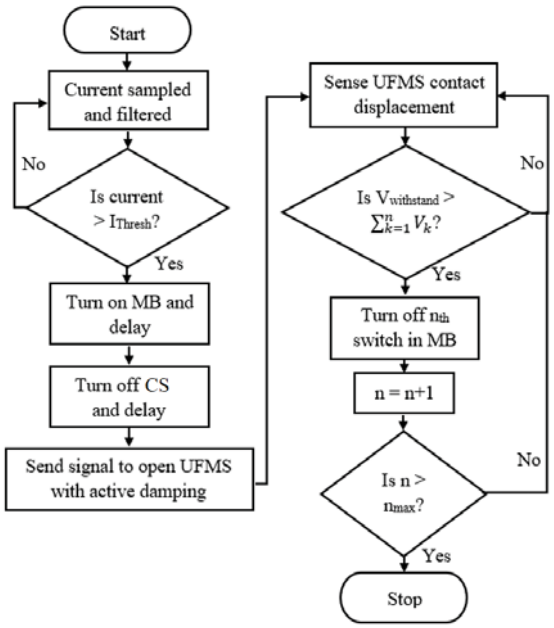

Fig. 12. Control logic flowchart for progressive shutdown

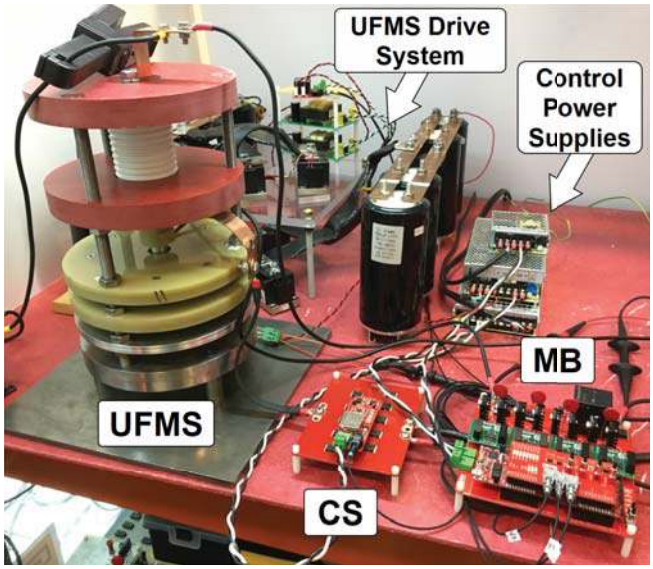

Fig. 13. Progressively switched, actively damped UFMS, hybrid DCCB test prototype

The DSP controller can implement dielectric strength coordination with two different switching control algorithms. First, static switching control operates the MB stages based on preset time values according to the operation characteristics of the UFMS for a low computational cost. Alternatively, dynamic switching control is implemented by actively sensing the displacement of the UFMS position sensor and the voltage differential across the MB in real-time. The DSP determines if adequate dielectric strength has been established to switch off the next sequential stage of the MB. With this same mechanism, restrike and arcing can be detected in the vacuum operator by the differential voltage sensors and action can be taken to prevent damage to the UFMS.

Communication between the subsystems of the hybrid DCCB is via fiber optic link to minimize signal latency and provide electric isolation between the subsystems. In this prototype, the DSP board is housed directly on the progressively switched MB and fiber optic links are connected to the UFMS driver system and the CS gate drivers, respectively.

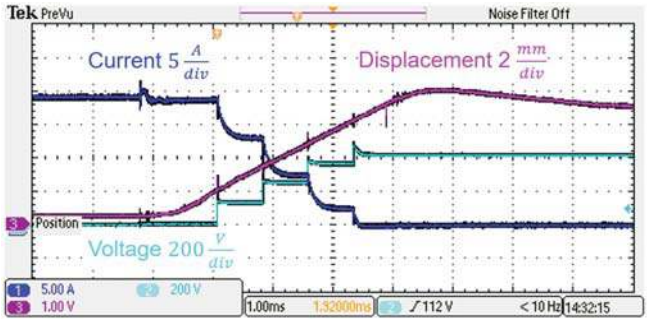

Fig. 14. Current, voltage and displacement waveforms from progressive hybrid test

V. Experimental Results

The test prototype that is shown in Fig. 13 was tested under the conditions listed in Table II to validate analytical and computer simulation validating their accuracy. Experimental voltage and current waveforms of the four-stage progressively switched, actively damped hybrid DCCB are shown in Fig. 14 and Fig. 15, and key testing parameters are listed in Table III.

TABLE. II. Progressively switched hybrid DCCB parameters

Component	Parameter	Units
V_{source}	425	V_{DC}
I_{load}	20	A_{DC}
R_{load}	20	Ω
L_{line}	2.5	mH
$V_{varistor}$	$100-120$	V_{DC}
$V_{clamping}$	175	V_{DC}

TABLE. III. Progressively switched hybrid DCCB test results

Metric	Progressively Switched	Single-Stage	Units
$t_{isolation}$	3.31	4.23	ms
$E_{absorbed}$	2.52	7.21	J

In this first generation prototype, the CS and UFMS are rated for higher currents and voltages than the MB as a proof of concept. The test was operated on a per unit basis to show the current curtailment during isolation and coordination of the dielectric strength of the UFMS and progressively switched MB. Additionally, it was tested under static conditions, as shown in Table II, Fig. 14, and Fig. 15. Continued validation of progressive switching will be demonstrated by performing fault isolation during a short circuit event and developing a second-generation MVDC device.

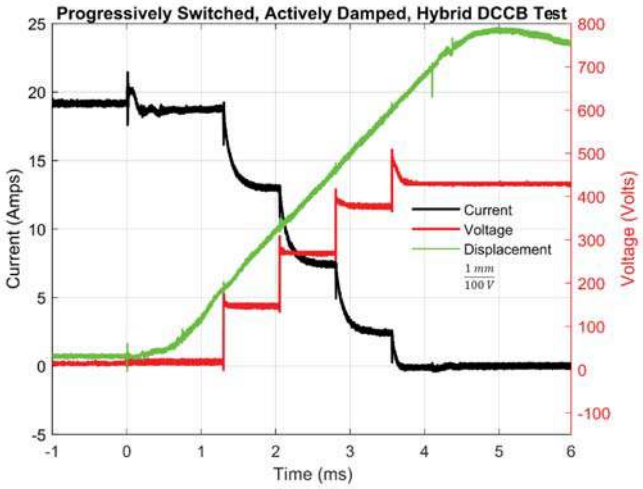

Fig. 15. Current, voltage and displacement waveforms from progressive hybrid test, processed for clarity

VI. Conclusions and Summary

A *Progressively Switched, Actively Damped, Hybrid DCCB* was presented with design and operational details coupled with analysis and computer simulation based modeling. A prototype was fabricated and tested to validate the analytical and computer models. This new hybrid DCCB design coordinates the voltage potential exerted across the solid-state switches of the hybrid DCCB with the UFMS displacement corresponding to the dielectric strength of the vacuum interrupter. A four-stage test prototype hybrid DCCB validated PSCAD and PLECS models and component controls. This novel design allows the solid-state switches to curtail fault current intermittently during UFMS opening operation by progressively switching off separate stages. It facilitates DCCB design with smaller, less expensive components and naturally balances the voltage differential across series connected power semiconductor devices. The progressive switching method requires less energy dissipation in the surge arrestor network, prolonging the life of the devices, minimizing system stress, and isolating fault current fast. The switching method proposed improves system stability by preventing voltage collapse in distribution systems supplied by converters.

The four-stage progressively switched hybrid DCCB shortens fault isolation time by 1.3 ms in simulation and 0.9 ms in the first generation prototype. It also reduces fault current by 175%, and requires devices with 45% the blocking voltage of single-stage DCCBs for the same isolation capability. Progressive switching can be readily applied to other existing hybrid DCCB designs to enable faster isolation of DC faults and limitation of peak fault current. Through progressive switching, we further enable MVDC distribution in residential microgrids, DC ships, data centers, and other applications. DC faults are isolated faster while placing less voltage strain on DCCB components using progressive switching, facilitating the use of smaller and more efficient devices to reduce cost and size while maximizing the benefits of the hybrid DCCB design.

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