Improved Common Mode Noise Models For Three Level T-Type Neutral Point Clamped Converters

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***Abstract*—Three level T-type based converter ($3LT^2C$) is becoming an attractive option in several grid connected power electronic applications as it offers several advantages like high efficiency, lower active component count compared to other three level converters and superior output ac voltage quality. Common mode (CM) based noise modeling for $3LT^2C$ has not been thoroughly explored in literature. This work presents an improved CM noise model for a grid connected $3LT^2C$ with an LCL filter. It is shown that the $3LT^2C$ has two high frequency CM noise sources which are responsible for ground leakage current injection. The effect of both CM noise sources on the overall CM model has been examined under different switching frequencies using sine triangle pulse width modulation (SPWM). Along with detailed analysis, extensive simulation results have been provided to validate the presented CM noise model.**

***Index Terms*—Common mode (CM) noise, CM filter, Electromagnetic Interference (EMI), Electromagnetic Compatibility (EMC), T-type inverter, voltage source inverter.**

I. Introduction

Over the last few years, three level neutral point based voltage source converters have become very popular for a variety of power electronic applications like renewable energy integration, traction systems, motor drive applications, data center applications, electric vehicle systems etc. This can be attributed primarily to better ac output voltage waveform quality and higher efficiency with increasing switching frequency [1]. Due to more number of steps in the output instantaneous voltage level in a three level converter, the harmonics in the output voltage are minimized leading to size reduction of the differential output filter. Amongst the different types of three level converters, the T-type based converter ($3LT^2C$) is fast becoming a favored option for low voltage applications as it has a lower active component count and higher efficiencies [2], [3].

Electromagnetic interference (EMI) typically occurs due to the high voltage slew rates or dv/dt during the switching transitions of the power semiconductor devices used for realizing the switching converters. EMI can be broadly categorized as differential mode (DM) and common mode (CM) noise emissions. CM models need to be developed for evaluating the CM currents (ground leakage currents) flowing through parasitic impedances referenced to ground or power earth in such switching converters and the associated EMI. The CM current path for a grid connected voltage source converter (VSC) has been illustrated in Fig. 1. The cumulative parasitic capacitance of the VSC to ground has been represented as C_p. A line impedance stabilization network (LISN) is typically used for EMI noise signature measurement of the equipment under test (EUT), in this case a VSC. Developing CM models in principle involves identifying the CM noise sources and all ground referenced parasitic capacitances associated with the switching converter. Most of the CM noise modeling and CM-EMI mitigation techniques have been proposed predominately for two level converters [4]–[6]. Development of CM noise models for three level converters, specifically CM modeling of $3LT^2C$, is still an active area of research. Though some EMI models have been explored for three level converters, most of them consider a single CM noise source [7]–[10]. While [11] does present a model with multiple CM noise sources, it is valid only for a three level diode clamped neutral point converter.

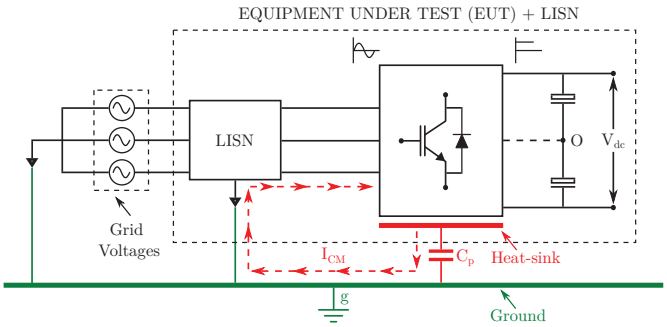

Fig. 1: The CM current path for a grid connected voltage source converter (VSC) under test.

This paper introduces an improved CM noise model for a grid connected $3LT^2C$ and shows the presence of two high frequency CM noise sources which contribute towards ground leakage currents. The paper has been organized as follows: The analysis and derivation for the CM noise model for $3LT^2C$ has been presented in Section II. The proposed CM noise model has been validated using switching simulations and it is compared with the conventional CM noise model in Section III. Section IV investigates the ground leakage currents due to individual CM noise sources. The simulation results detailing

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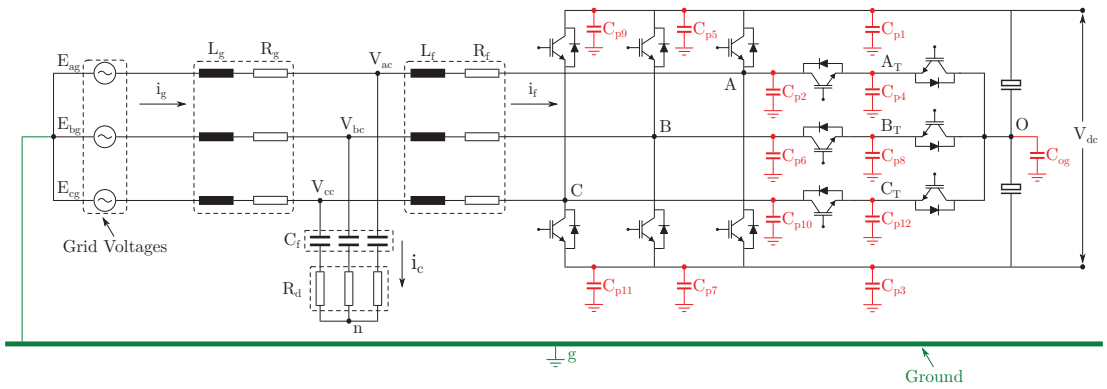


Fig. 2: A three level T-type based grid connected converter with associated ground parasitic capacitances. For the CM noise model derivation, the LISN has not been shown for clarity purposes.

CM-EMI noise signatures of $3LT^2C$ have been depicted in Section V.

II. EMI Noise Model Derivation for Three Level T-Type Converter

Fig. 2 shows a three level T-type converter with all the different parasitic capacitances associated with the converter. The heat-sink of the converter is assumed to be grounded for the presented analysis. C_{p1}, C_{p5}, C_{p9} represent the capacitances between the high side switching devices and heat-sink while C_{p3}, C_{p7}, C_{p11} delineate the low side switching device to ground capacitances. The DC link mid-point to ground capacitance is represented by C_{og}. It can be observed that values of C_{p4}, C_{p8}, C_{p12} can be different than that of the other parasitic capacitances since there are 2 neutral point clamped switching devices connected in an anti-serial configuration to each phase leg. The two semiconductor devices can be connected in a common drain / collector or common source / emitter configuration as shown in Fig. 3. The common drain / collector configuration as compared to that of common source / emitter is more popular due to the fact that it requires one less isolated gate drive supply per phase leg. The actual values of the parasitic capacitances depend on the structure and packaging of the semi-conductor switches or modules as well as heat-sink to ground or heat-sink to enclosure connections.

To obtain the complete CM noise model for T-type converter, all possible dv/dt nodes caused due to high frequency switching of the semiconductor switches have to be analyzed and taken into account. From Fig. 2, it can be observed that for each leg of the converter there exists two dv/dt nodes which correspond to the instantaneous per phase node and the node between the two semi-conductor switches connecting each phase to the DC link midpoint.

For deriving the necessary CM equations, the three level T-type converter is assumed to be operating as a rectifier with ac side current control. KVL can be used to derive a relationship between the grid voltages and the instantaneous per phase voltages of $3LT^2C$ as shown in (1).

$$\begin{cases} E_{ag} = L_g\dfrac{di_{ag}}{dt} + L_f\dfrac{di_{af}}{dt} + i_{ag}R_g + i_{af}R_f + V_{AO} + V_{Og} \\ E_{bg} = L_g\dfrac{di_{bg}}{dt} + L_f\dfrac{di_{bf}}{dt} + i_{bg}R_g + i_{bf}R_f + V_{BO} + V_{Og} \\ E_{cg} = L_g\dfrac{di_{cg}}{dt} + L_f\dfrac{di_{cf}}{dt} + i_{cg}R_g + i_{cf}R_f + V_{CO} + V_{Og} \end{cases} \tag{1}$$

Adding all the grid voltages and assuming balanced conditions ($E_{ag} + E_{bg} + E_{cg} = 0$) leads to a per phase equivalent equation as shown below.

$$\begin{aligned} 0 = \frac{1}{3}L_g\frac{(di_{ag} + di_{bg} + di_{cg})}{dt} + \frac{1}{3}L_f\frac{(di_{af} + di_{bf} + di_{cf})}{dt} \\ + \frac{1}{3}R_g(i_{ag} + i_{bg} + i_{cg}) + \frac{1}{3}R_f(i_{af} + i_{bf} + i_{cf}) + V_{CM1} + V_{Og} \end{aligned} \tag{2}$$

V_{CM1} refers to the CM voltage produced due to the per phase

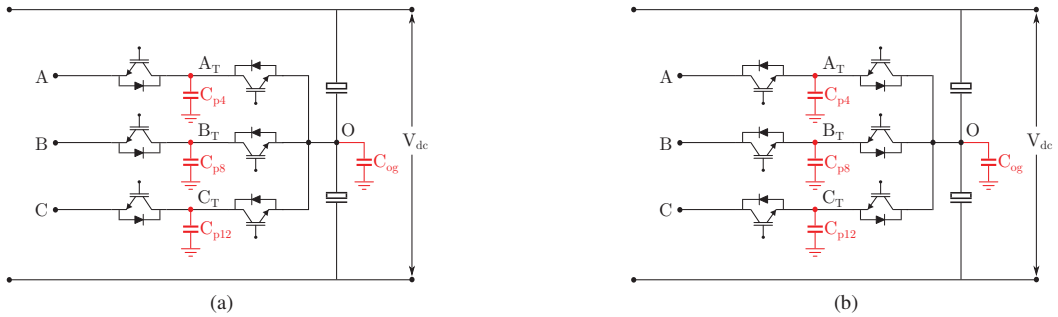


Fig. 3: Anti-serial switch configuration (IGBT / MOSFET) (a) common collector / drain and (b) common emitter / source.

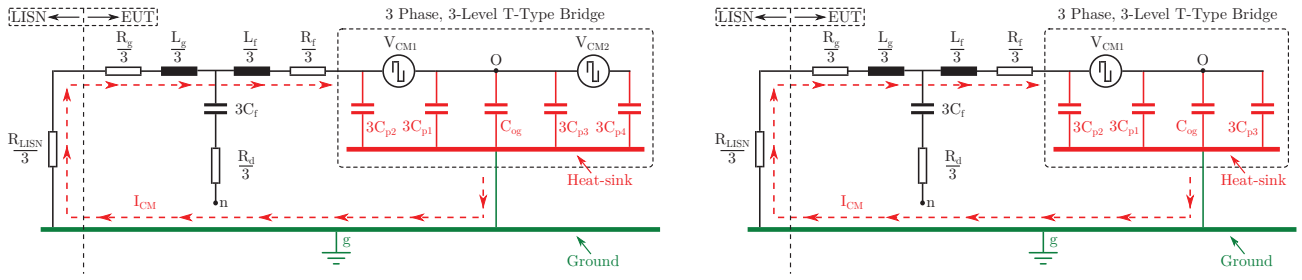


Fig. 4: CM noise models for three level, 3ϕ T-type based grid connected converter (a) proposed CM noise model (b) conventional CM noise model [9], [10]. The measured parasitic capacitances of all the 3 legs of the converter were found to be similar and are mentioned in Table I.

instantaneous voltages and can be described by (3).

$$V_{CM1} = \frac{(V_{AO} + V_{BO} + V_{CO})}{3} \tag{3}$$

Equation (4) relates the grid voltages and the ac side capacitors of the LCL filter where V_{ac}, V_{bc} and V_{cc} refer to phase voltages across the ac capacitors and damping resistors.

$$\begin{cases} E_{ag} = L_g \dfrac{di_{ag}}{dt} + i_{ag}R_g + V_{ac} + V_{ng} \\ E_{bg} = L_g \dfrac{di_{bg}}{dt} + i_{bg}R_g + V_{bc} + V_{ng} \\ E_{cg} = L_g \dfrac{di_{cg}}{dt} + i_{cg}R_g + V_{cc} + V_{ng} \end{cases} \tag{4}$$

Again, assuming balanced grid voltages ($E_{ag}+E_{bg}+E_{cg} = 0$) equation (4) can be simplified as shown in (5).

$$0 = \frac{1}{3}L_g \frac{(di_{ag} + di_{bg} + di_{cg})}{dt} + \frac{1}{3}R_g(i_{ag} + i_{bg} + i_{cg}) + V_{Ccom} + V_{ng} \tag{5}$$

Equation (6) can be arrived at by writing a set of KCL equations at the ac capacitor nodes (of the LCL filter).

$$\begin{cases} i_{ag} = i_{ac} + i_{af} \\ i_{bg} = i_{bc} + i_{bf} \\ i_{cg} = i_{cc} + i_{cf} \end{cases} \tag{6}$$

Adding the grid side currents, $i_{ag} + i_{bg} + i_{cg}$ leads to (7) and (8).

$$\begin{aligned} i_{Ccom} &= i_{gcom} - i_{fcom} = i_{ac} + i_{bc} + i_{cc} \\ &= C_f \frac{d(V_{acap} + V_{bcap} + V_{ccap})}{dt} = \frac{(V_{ar} + V_{br} + V_{cr})}{R_d} \\ &= 3C_f \frac{dV_{Ccap}}{dt} = \frac{3V_{Cr}}{R_d} \end{aligned} \tag{7}$$

$$\begin{aligned} V_{Ccom} &= \frac{(V_{ac} + V_{bc} + V_{cc})}{3} \\ &= \frac{(V_{acap} + V_{bcap} + V_{ccap})}{3} + \frac{(V_{ar} + V_{br} + V_{cr})}{3} \end{aligned} \tag{8}$$

V_{acap}, V_{bcap}, V_{ccap} and V_{ar}, V_{br}, V_{cr} refer to the voltages across the ac capacitors and damping resistors respectively. To analyze the dv/dt node between the anti-serial connected neutral point clamped devices, the following equations shown in (9) can be written. V_{A_TO}, V_{B_TO} and V_{C_TO} denote the voltages appearing across the dc link midpoint, O and C_{p4}, C_{p8} and C_{p12} respectively.

$$\begin{cases} V_{cp4} = V_{A_TO} + V_{Og} \\ V_{cp8} = V_{B_TO} + V_{Og} \\ V_{cp12} = V_{C_TO} + V_{Og} \end{cases} \tag{9}$$

Adding the voltages, $V_{cp4} + V_{cp8} + V_{cp12}$ leads to (10) which describes the second CM noise source.

$$\frac{(V_{cp4} + V_{cp8} + V_{cp12})}{3} = V_{CM2} + V_{Og} \tag{10}$$

V_{CM2} is the CM voltage applied to all the ground referenced parasitic capacitances (C_{p4}, C_{p8} and C_{p12}) of the neutral point clamped switching devices and is defined as shown in (11).

$$V_{CM2} = \frac{(V_{A_TO} + V_{B_TO} + V_{C_TO})}{3} \tag{11}$$

Using equations (2), (3), (7) and (11) the overall CM noise model of $3LT^2C$ can be arrived at as shown in Fig. 4a. For EMI measurements, typically a LISN is used and its resistance, R_{LISN} across which the CM noise is measured has also been shown. Hence, it is observed the CM noise model for a three level T-type converter contains two high frequency CM noise sources. The LCL filter behaves like an L filter in the CM equivalent noise model since secondary of the ac capacitors is floating with respect to ground. As a reference, the conventional CM noise model described in [9], [10] has been illustrated in Fig. 4b for the sake of comparative evaluation.

III. Validation of Proposed CM Noise Model

To validate the accuracy of the proposed CM noise model, three IGBT based T-type modules (SKiM601TMLI12E4B) were selected for extracting the parasitic capacitance information. The measured parasitic capacitance values are given in Table I.

A switching simulation of a three level, 3ϕ grid connected $3LT^2C$ converter was developed to compare the performance of proposed and conventional CM noise models presented in Fig. 4. Sine-triangle pulse width modulation (SPWM) scheme was used to generate the gate pulses for the semi-conductor

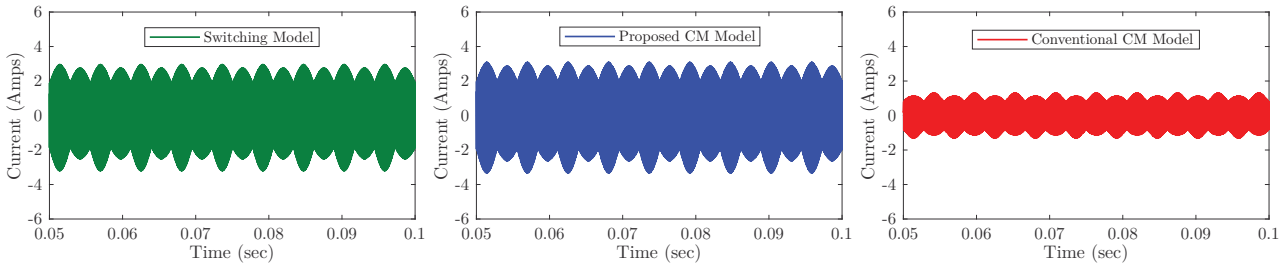


Fig. 5: Comparison between ground leakage current (I_{CM}) measured from (a) switching model and (b) proposed CM noise model and (c) conventional CM noise model with sine triangle modulation (SPWM) and switching frequency, $f_{sw} = 40\ kHz$.

TABLE I: Measured Parasitic Capacitances

Parameter	Value
$C_{p1} \approx C_{p5} \approx C_{p9}$	$1.428\ nF$
$C_{p3} \approx C_{p7} \approx C_{p11}$	$1.405\ nF$
$C_{p2} \approx C_{p6} \approx C_{p10}$	$1.489\ nF$
$C_{p4} \approx C_{p8} \approx C_{p12}$	$1.420\ nF$
C_{og}	$4.071\ nF$

TABLE II: Three level T-type Converter Parameters

Parameter	Value
Grid voltage, V_g	$120\ V$
Grid frequency, f_g	$60\ Hz$
DC link capacitance, C	$220\ uF$
AC filter inductance, $L_g = L_f$	$1\ mH$
AC filter resistance, R_L	$0.2\ \Omega$
Damping resistance, R_d	$10\ \Omega$
LISN resistance, R_{LISN}	$50\ \Omega$
Switching frequency, f_{sw}	$10\ kHz\ -\ 40\ kHz$
DC link voltage, V_{dc}	$400\ V$

devices. The circuit parameters used in simulation have been provided in Table. II.

The ground leakage currents from the switching and CM simulation models are depicted in Fig. 5 corresponding to a switching frequency of $40\ kHz$. It can be observed from Fig. 5 that the ground leakage current (I_{CM}) from the proposed CM model matches accurately with that of the switching model thereby validating the proposed CM model. On the contrary, the ground leakage current predicted by the conventional CM model is much smaller in magnitude. This shows the importance of the second noise source, V_{CM2} on the ground leakage current of a T-type converter.

IV. Effect of CM Noise Sources in $3LT^2C$

In the previous section, the need for accurate modeling of two CM noise sources in a $3LT^2C$ has been established. It is important to understand the CM contribution of each noise source independently as this information could be used to select an appropriate modulation strategy for $3LT^2C$.

The ground leakage current produced due to both the high frequency CM noise sources can be determined by examining the passive network of the proposed CM noise model and can be qualitatively analyzed based on the corresponding frequency domain impedance or admittance plots. Further, the ground leakage current contributions due to the two CM noise sources can be ascertained separately by applying superposition principle on Fig. 4a to obtain two individual models as shown in Fig. 6a and 6b. By solving for the ground leakage current in Fig. 6a and 6b, the leakage current contribution of V_{CM1} and V_{CM2} can be assessed.

The circuits depicted in Fig. 6a and 6b have been simulated to showcase the individual leakage current contributions due to the two noise sources, V_{CM1} and V_{CM2}. The overall ground leakage current from the proposed model is showcased in Fig.

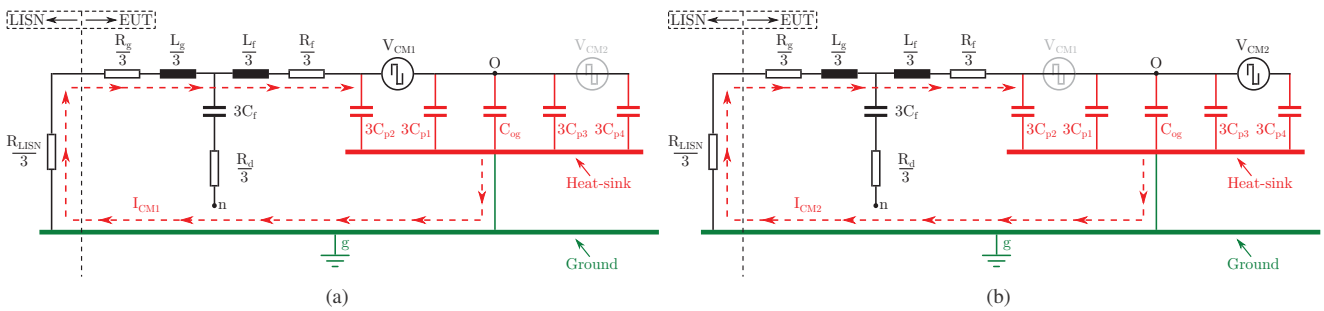
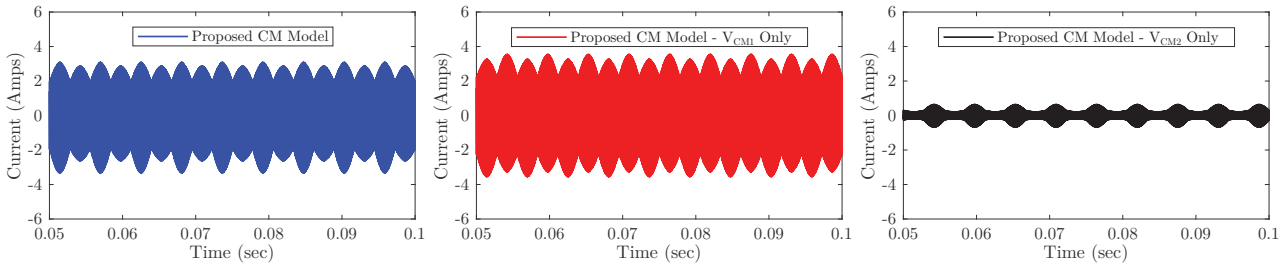


Fig. 6: Ground leakage currents due to (a) CM noise source 1 (V_{CM1}) and (b) CM noise source 2 (V_{CM2}).



(a) (b) (c)

Fig. 7: Ground leakage currents (I_{CM}) measured from (a) proposed CM noise model (b) proposed CM noise model with V_{CM1} only and (c) proposed CM noise model with V_{CM2} only.

7a and the individual leakage current contributions from each CM noise source, V_{CM1} and V_{CM2} are depicted in Fig. 7b and Fig. 7c respectively. It can be seen from Fig. 7a and Fig. 7b that the ground leakage current produced due to only V_{CM1} is actually greater than the overall leakage current produced by both the noise sources for the chosen operating condition with sine triangle modulation. This also reinforces the fact that accounting for all the noise sources plays an important role in determining the amplitude and frequencies of the ground leakage current.

V. Results and Discussion

In Section III, it was demonstrated that the proposed model predicts different results in terms of the ground leakage current as compared to the conventional model and this can be attributed to the second noise source. The differences between the proposed model and conventional model are further explored by sweeping the switching frequency from 10 kHz to 40 kHz.

A. Ground leakage current comparison

The ground leakage current from the proposed model is compared with that of the conventional model in Fig. 8 as the switching frequency is varied. For a given value of parasitic capacitances and circuit parameters as defined in Table. I and Table. II, the differences between the two models are more pronounced at higher switching frequencies with sine-triangle based modulation strategy. The circuit simulation results corresponding to 10 kHz, 20 kHz and 40 kHz operation are captured in Fig. 8a, Fig. 8b and Fig. 8c respectively.

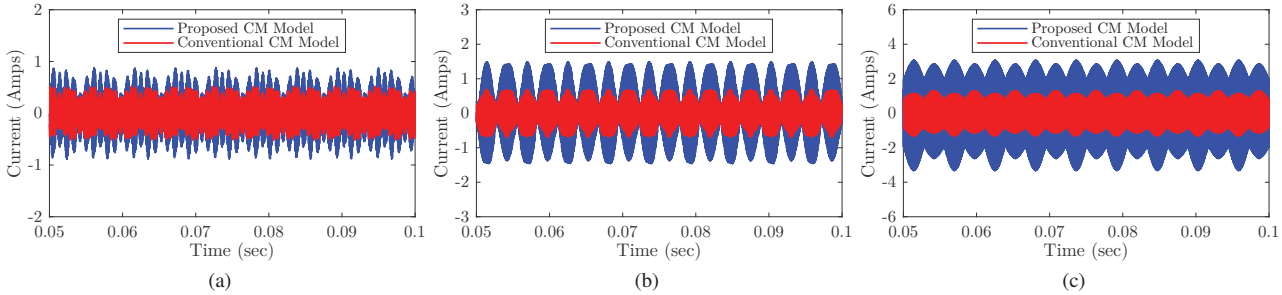
B. CM noise comparison

Another important factor that needs to be compared is the CM noise levels with the proposed and conventional model. The CM filter is typically sized to offer a certain attenuation to switching frequency CM noise and its harmonics to ensure EMI compliance in the conducted emission band (150 kHz – 30 MHz). The way in which the CM noise gets modeled can impact the CM filter sizing.

TABLE III: Measure of CM Noise (V_{LISN})

Switching Frequency, f_{sw}	Proposed Model	Conventional Model
10 kHz	5.07V	2.94V
20 kHz	11.15V	4.12V
40 kHz	30.90V	12.34V

Fig. 9a, Fig. 9b and Fig. 9c depict the CM noise as seen across the LISN resistance. It can be discerned that the CM noise levels are different with the proposed model versus the conventional model due to the presence of a second noise source. In order to quantify the differences between the two models, the rms value of the CM voltage seen across the LISN resistance is tabulated in Table. III. The differences



(a) (b) (c)

Fig. 8: Effect on ground leakage current (I_{CM}) due to variation in switching frequency, f_{sw} where (a) $f_{sw} = 10\ kHz$ (b) $f_{sw} = 20\ kHz$ and (c) $f_{sw} = 40\ kHz$ using sine triangle modulation (SPWM).

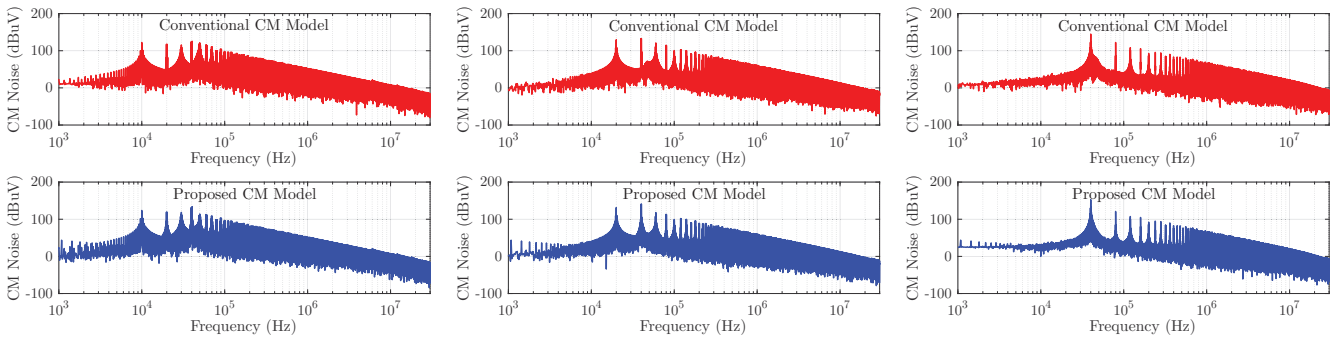


Fig. 9: CM noise comparison between proposed and conventional CM models when (a) $f_{sw} = 10\ kHz$ (b) $f_{sw} = 20\ kHz$ and (c) $f_{sw} = 40\ kHz$ using sine triangle modulation (SPWM).

between the two models get more pronounced as the switching frequency increases. Though the major difference is introduced by the switching frequency component, the CM filter sizing requirement predicted by the proposed model is slightly higher than that predicted by the conventional model. This can become a serious concern if the switching frequency increases beyond $150\ kHz$ as the CM filtering requirements could be $3-5$ times higher than what is predicted by the conventional model. This underlines the need for improved CM noise models for multilevel converters where all the noise sources are accounted for as in the proposed example of a $3LT^2C$.

VI. Conclusion

An improved CM noise model has been proposed and analyzed for the grid connected three level, 3ϕ T-type converter ($3LT^2C$). The CM noise model was developed by accounting for the LCL filter as well as the device to heat-sink / ground parasitic capacitances associated with semiconductor switches. It is delineated that the $3LT^2C$ contains two high frequency CM noise sources which are responsible for the ground leakage current injection. The effect of each noise source on the ground current contribution has been evaluated with the help of superposition principle. The effectiveness of the proposed CM model is validated by comparing it with a switching simulation of $3LT^2C$. The conventional CM model reported in literature is not able to accurately quantify the leakage current or conducted emission spectra as the effect of one noise source is ignored. Ground leakage currents and CM-EMI noise signatures have been simulated for both the proposed and conventional CM models for different switching frequencies to showcase the limitations of conventional model.

References

[1] J.-S. Lai and F. Z. Peng, "Multilevel converters-a new breed of power converters," *IEEE Transactions on Industry Applications*, vol. 32, no. 3, pp. 509–517, May 1996.

[2] M. Schweizer and J. W. Kolar, "Design and implementation of a highly efficient three-level t-type converter for low-voltage applications," *IEEE Transactions on Power Electronics*, vol. 28, no. 2, pp. 899–907, Feb 2013.

[3] M. Schweizer, T. Friedli, and J. W. Kolar, "Comparative evaluation of advanced three-phase three-level inverter/converter topologies against two-level systems," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 12, pp. 5515–5527, Dec 2013.

[4] D. Gonzalez, J. Gago, and J. Balcells, "New simplified method for the simulation of conducted emi generated by switched power converters," *IEEE Transactions on Industrial Electronics*, vol. 50, no. 6, pp. 1078–1084, Dec 2003.

[5] J.-S. Lai, X. Huang, E. Pepa, S. Chen, and T. W. Nehl, "Inverter emi modeling and simulation methodologies," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 3, pp. 736–744, June 2006.

[6] E. Gubia, P. Sanchis, A. Ursua, J. Lopez, and L. Marroyo, "Frequency domain model of conducted emi in electrical drives," *IEEE Power Electronics Letters*, vol. 3, no. 2, pp. 45–49, June 2005.

[7] M. C. Cavalcanti, A. M. Farias, K. C. Oliveira, F. A. S. Neves, and J. L. Afonso, "Eliminating leakage currents in neutral point clamped inverters for photovoltaic systems," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 1, pp. 435–443, Jan 2012.

[8] L. Wang, Y. Shi, Y. Shi, R. Xie, and H. Li, "Ground leakage current analysis a suppression in a 60-kw 5-level t-type transformerless sic pv inverter," *IEEE Transactions on Power Electronics*, vol. 33, no. 2, pp. 1271–1283, Feb 2018.

[9] D. O. Boillat, F. Krismer, and J. W. Kolar, "Emi filter volume minimization of a three-phase, three-level t-type pwm converter system," *IEEE Transactions on Power Electronics*, vol. 32, no. 4, pp. 2473–2480, April 2017.

[10] M. Hartmann, H. Ertl, and J. W. Kolar, "Emi filter design for a 1 mhz, 10 kw three-phase/level pwm rectifier," *IEEE Transactions on Power Electronics*, vol. 26, no. 4, pp. 1192–1204, April 2011.

[11] H. Zhang, L. Yang, S. Wang, and J. Puukko, "Common-mode emi noise modeling and reduction with balance technique for three-level neutral point clamped topology," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 9, pp. 7563–7573, Sept 2017.