Y9.ET3: Robust Gen-III SST Development

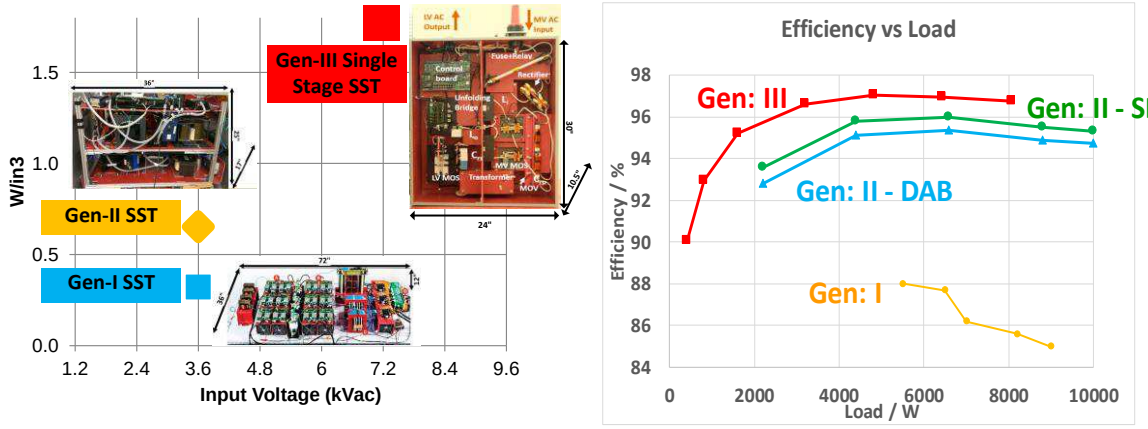
Project Leaders: Alex Huang (ECE/NCSU)

Students: Li Wang (PhD), Qianlai Zhu (PhD)

Industrial Champions: Wolfspeed (devices)

1. Project Goals

The overall objective of this project is to improve the ruggedness, efficiency and power density of the single phase 7.2 kV, 20kVA Solid State Transformer (SST). To further increase the efficiency while attaining small size volume, Gen-III SST adopted a single stage AC-AC conversion techniques based on 15kV SiC devices. To our knowledge, this is the only known effort in the world on direct medium voltage AC-AC conversion. Bulk capacitance used in Gen-I and Gen-II are eliminated. Only two high voltage high frequency devices are required in the whole system. Comparing with Gen-II SST, the overall Gen-III AC-AC system attained a power density three times higher as shown in Fig. 1 (a). Fig. 1 (b) shows the efficiency curves of Gen-I, Gen-II and Gen-III SST. Gen-II obtains 97% efficiency at heavy load conditions, which is 2% higher than Gen-II.



(a) (b)

Figure. 1 Comparison of Gen-I, Gen-II and Gen-III SST (a) Power density versus input voltage; (b) Efficiency versus load conditions

2. Role in Support of Strategic Plan

As a key enabling technology platform, the SST serves as a platform for fundamental science technologies such as Post Silicon Devices developed in the center and by industry partner Cree. It also provides DC and AC interfaces for center developed DESDs, DRERs and smart loads. The Si-IGBT based multi-level Gen-I SST and 15kV SiC-MOSFET based Gen-II SST have been developed and delivered as revolutionary smart interfaces at 3.6kV and 10 kW level in the previous years. According to the strategic research roadmap and the feedback from the Y8 site visit team, the role of the Gen III SST is to improve efficiency, and robustness, as well as to reach an input voltage 7.2 kV level.

3. Fundamental Research Barriers and Methodologies Used to Address Them

The main challenges for this Gen-III SST project are to develop reliable, high power density, efficient and cost-effective power electronics for the 7.2kV smart grid applications. Since the power and voltage level are twice as Gen-II SST, research barriers related to high voltage (7.2 kV AC) solid state power conversion need to be addressed: 1) Reliable system control scheme that can cover all the operation scenarios

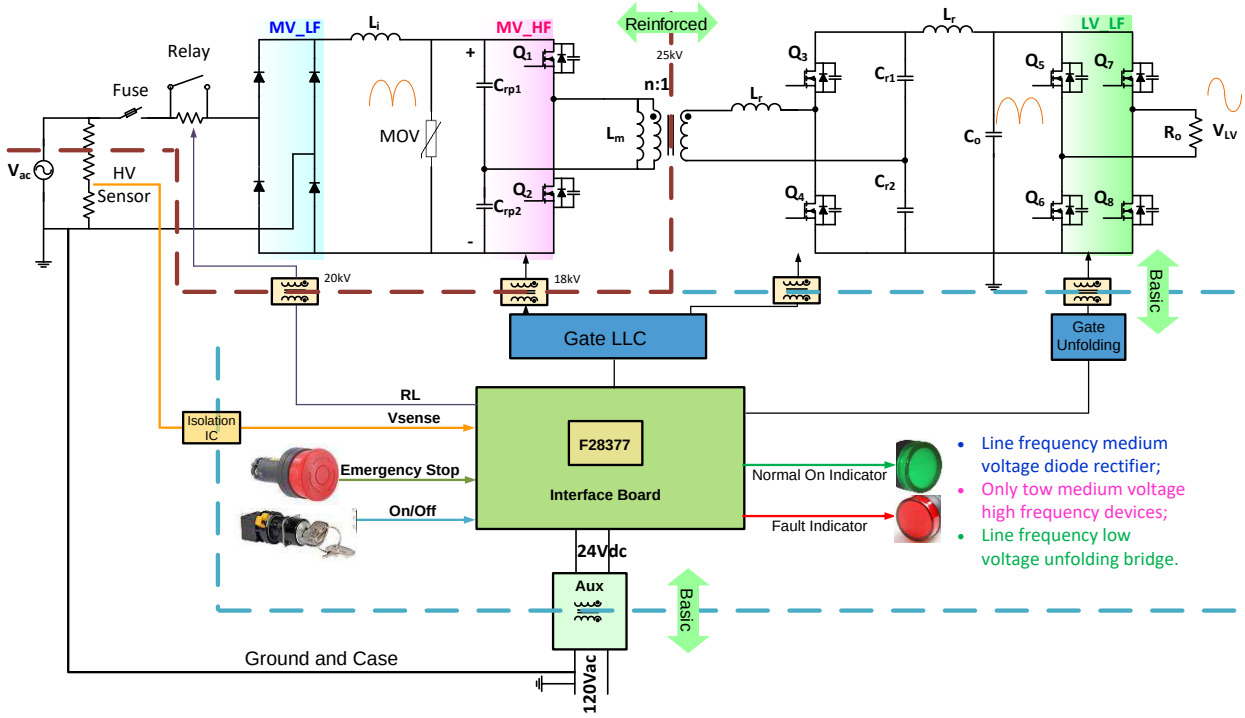
including soft start up, normal operation, protection and recover from fault status; 2) Over all system package that can handle > 10 kV voltage stress. 3) Due to the significant amount of energy stored in parasitic capacitors, hard switching devices might be over heated when switching frequency is over 10 kHz. Soft switching of all the 15 kV SiC semiconductors are mandatorily required for ruggedness as well as efficiency consideration. In this project, all medium voltage medium frequency switches have achieved zero voltage switching from zero to full load. 4) In order to realize three stage AC-AC conversion, at least six 15 kV SiC devices are needed in both Gen I and Gen II SST. High cost as well as relatively high power loss make SST less competitive compared to traditional line frequency transformer. This year, a single stage AC-AC resonant converter is adopted. Only two 15 kV SiC devices are needed. System efficiency is also improved due to the less number of power stage.

4. Achievements in Previous Years with an Emphasis on the Current Year

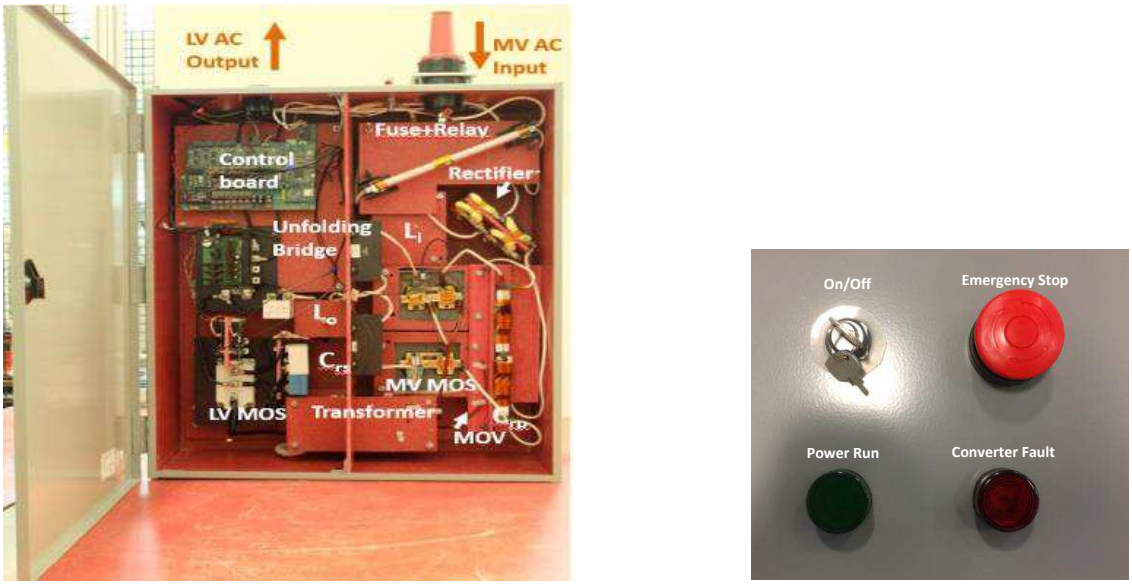
In the previous three years, the team reported that an overall efficiency of 95% for three power stages at 10kW power level and 3.6kV RMS grid voltage were successfully achieved and demonstrated in Gen-II SST. In the current year, the achievements so far are a Gen-III SST with direct AC-AC conversion at 40 kHz, and an efficiency higher than 97%. These major achievements are summarized below.

4.1 System Diagram and Hardware

Figure.2 (a) shows the diagram of the Gen-III SST. Advanced transformer and other high insolation techniques are adopted to provide galvanic isolation between medium voltage (MV) side and low voltage (LV) side. The whole system contains only two MV high frequency devices Q_1 and Q_2. The controller system is based on TI digital controller IC TMS320F28377D. In Figure.2 (b), the system hardware setup is shown. MV voltage and fuse are implemented to protect the system from fault conditions. The whole system is very compact. Operation panel depicted in Figure.2 (c) contains one on/off switches, one emergency stop switches and two system status LED indicators.



(a)



(b) (c)

Fig. 2 (a) System diagram (b) system hardware (c) switches and signal indicators

4.2 Metal Oxide Varistors (MOV) for Over Voltage Protection

To protect the SST III from MV grid over voltage conditions such as surge or EFT, MOV is implemented in the system. As shown in Fig. 3 (a), three MOVs are connected in series to achieve high voltage operation ability. Fig. 3 (b) shows the proposed MOV leakage current versus the voltage. When the voltage is lower than 5.5kV, the MOV draws very small leakage current and is on off status. When the voltage is higher than 6kV, the leakage current increase rapidly, which helps limit the voltage within 6kV and protect the system from over voltage conditions.

(a) (b)

Figure 3. (a) MOV over voltage protection hardware (b) MOV leakage current vs voltage

4.3 ZVS Operation and 15kV SiC MOSFET Utilization

There is a tradeoff between the magnetizing inductance and dead time for DC-DC resonant converter due to their conflicting effects on the conduction loss of the power switches. In the single-stage AC-AC SST, the design trade-off is not only related to the conduction loss but also switching loss since the resonant converter can't reach soft switching for an entire voltage range with fixed magnetizing inductance and dead time. In order to optimize the total loss on MV devices with constant deadtime strategy. Conduction loss and switching losses of the MV devices are calculated separately based on different L_m and deadtime values. Fig. 4 shows the overall semiconductor loss versus the magnetizing inductance and dead time. For high magnetizing inductance and short dead time, the overall loss is high due to large switching loss.

However, with low magnetizing inductance and long dead time, the overall loss increases due to the high conduction loss. Optimized parameters are chosen, such that low semiconductor loss can be achieved.

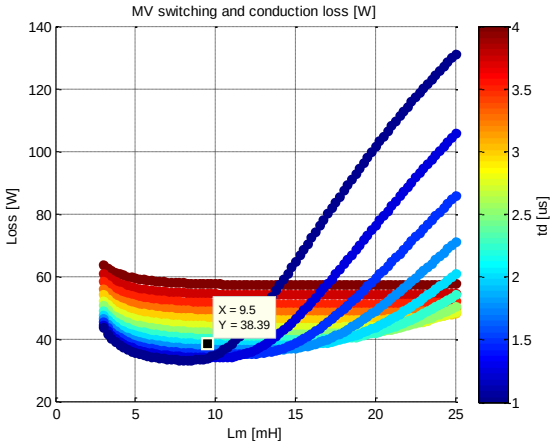
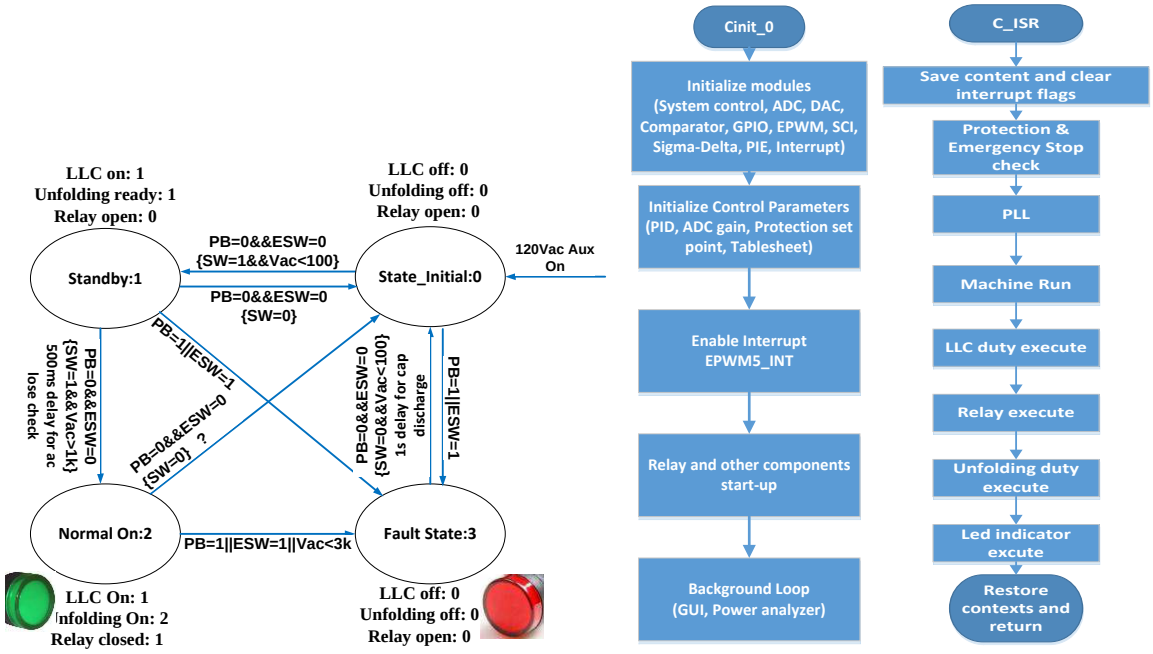


Fig. 4 Semiconductor losses vs magnetizing inductance and dead time.

4.4 System State Machine and Control Flow Chart

A good sequential control logic is also very important for the system to operate reliably. The states diagram and transition conditions of the system is depicted in Fig. 5 (a), which includes all the possible status of the system and all inside and outside signals that can be used to define and control the system operation. Transitions from one active state to another state if the transition condition is logic true. Code flow charts are also designed carefully and is shown in Fig. (b) (c).



(a) (b)

Figure. 5 (a) System state machine; (b) code flow chart

4.5 Experimental Results

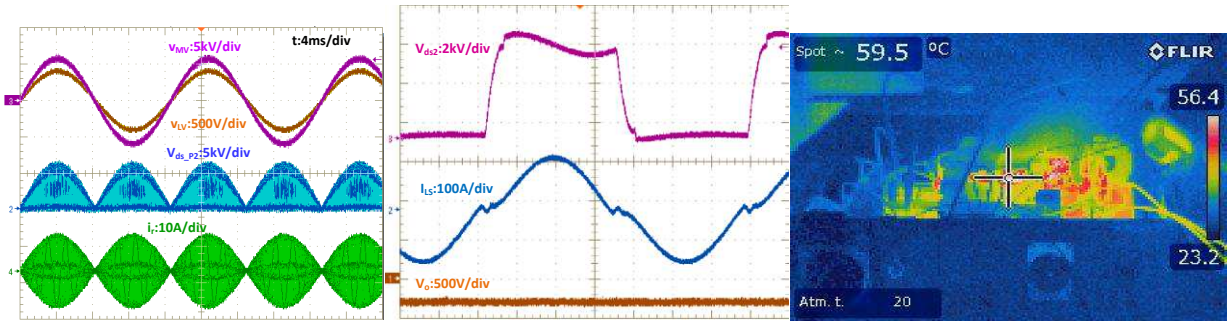
Gen-I and Gen-II both adopts multi-stage configuration as the structure, which consists of two medium frequency AC-DC power conversion stages and a medium frequency AC-AC conversion stage. This

approach can potentially achieve many attractive features such as Var compensations, voltage regulation, fault isolation and bidirectional power flow.

However, three stages of power conversion is the main drawback for multi-stage approach to achieve high efficiency. Moreover, this approach contains MV AC-DC stage that operates under hard switching condition. The significant turn-on losses caused by the parasitic output capacitance of the semiconductor devices limit the switching frequency which often leads to necessary additional bulk inductors and capacitors. MV relay combined with resistor is also needed on the MV side to limit the inrush current during start-up.

In Gen-III direct AC-AC SST, a galvanic isolated bidirectional AC-AC converter for medium voltage applications is proposed. CLLC-type resonant network is adopted in the MV MF stage since ZVS switching is easy to achieve during wide input voltage and load range, while attaining bidirectional power flow. 15kV SiC MOSFETs are studied and utilized with careful design to achieve switching frequency higher than 35kHz so that the size of passive components can be reduced. Moreover, there is no bulk DC capacitors in the proposed system, which further decreases the system volume and weight. The proposed SST has following functionalities 1) galvanic isolation with bidirectional power flow, 2) voltage regulation 4) 97% peak efficiency with 40kHz frequency operation, 5) inrush current limit and unity power factor.

The experimental results at 3.6k Vac to 240 Vac are illustrated in Figure. 6(a)(b). It can be seen from Figure. 6(b), that the soft switching is realized at full load operation. Figure. 6(a) shows the input and output has zero phase shift. Figure. 6(c) gives the thermal performance at 3.6kVac/240Vac, 8.8 kW condition, which shows a very good performance under room temperature and indicates potential higher power operation ability.



(a) (b) (c)

Figure. 6 Experimental results of proposed AC-AC SST (a) steady state operation waveforms (b) switching period operation waveforms (c) 8.8 kW thermal performance at 3.6kVac

5. **Other Relevant Work Being Conducted Within and Outside of the ERC**

   In Europe and China, there are many new activities underway to develop the SST for power grid, high-speed train, MV renewable energy system, electric vehicle charging stations, and others applications. There is a global rush to develop SST technology and FREEDM should be proud of being the key driving force behind it. Worldwide developments mostly take low voltage multilevel approach similar to the FREEDM Gen-I approach. Current FREEDM approach is therefore more fundamental and unique because it has the capability to deliver a much simpler and robust solution.

6. **Milestones and Deliverables**

   The expected milestones and deliverables of the SST in Year 9 are:

- Finish the development of the Gen-III direct AC-AC SST and its testing under 7.2kVac condition, particularly with increased power level and operation of SiC devices at elevated temperatures. Verification of Gen-III SST under the condition of the rated voltage and the rated power levels.

7. Plans for Next Five Years

- Improve the utilization of the SiC power devices in the SST by increasing its operation voltage and current and hence the thermal stress towards higher junction temperature operation. This will result in more compact and more cost effective SST design. This will be demonstrated through the development of a much more radically different Gen-IV SST
- Unique application opportunity for the SST such as MV charger or MV PV Inverter (as recommended by SST working group). Both examples are uni-directional SSTs.
- Knowledge dissemination through publications, technology transfer and commercialization

7. Member Company Benefits

Member companies will benefit from the optimized design and real implementation of >10kV SiC switches and improved MV topologies and practical design of the highly reliable and efficient single stage AC-AC converter with the highest switching frequency and >20 kV isolation capability. So far our development also benefits greatly from our partnership from Cree/Wolfspeed. All high voltage devices are provided by Cree.

8. Publications

1) A. Q. Huang, "Medium-Voltage Solid-State Transformer: Technology for a Smarter and Resilient Grid," in *IEEE Industrial Electronics Magazine*, vol. 10, no. 3, pp. 29-42, Sept. 2016. doi: 10.1109/MIE.2016.2589061
2) Li Wang; Qianlai Zhu; wensong Yu; Alex Huang "A Medium Voltage Medium Frequency Isolated DC-DC Converter Based on 15 kV SiC Mosfets"; IEEE Journal of Emerging and Selected Topics in Power Electronics; Year: 2016, Volume: PP, Issue: 99;Pages: 1 - 1, DOI: 10.1109/JESTPE.2016.2639381
3) A. Q. Huang, Li Wang, Q. Tian, Qianlai Zhu, Dong Chen and Wensong Yu, "Medium voltage solid state transformers based on 15 kV SiC MOSFET and JBS diode," *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*, Florence, 2016, pp. 6996-7002.
4) L. Wang, Q. Zhu, W. Yu, and A. Huang, “A study of dynamic high voltage output charge measurement for 15 kV SiC MOSFET,” in Proc. IEEE Energy Convers. Congr. Expo. (ECCE), Sep. 2016.
5) Q. Zhu, L. Wang, W. Yu, and A. Huang, “Medium Voltage AC-DC Rectifier for Solid State Transformer (SST) Based on an Improved Rectifier Topology,” in Proc. IEEE Energy Convers. Congr. Expo. (ECCE), Sep. 2016.
6) Q. Zhu, L. Wang, L. Zhang, W. Yu and A. Q. Huang, "Improved medium voltage AC-DC rectifier based on 10kV SiC MOSFET for Solid State Transformer (SST) application," *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, 2016, pp. 2365-2369.